

Simple Method for ADC Characterization under the Frame of Digital PM and AM Noise Measurement

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Abstract—The last years improvements of electronic circuits has allowed the appliance of digital systems in phase noise measurement techniques where low noise and high accuracy are required, yielding flexibility in the implementation and setup of measurement systems. By definition, any measure performed is always affected and limited by the noise of the measurement instrument itself. Considering that the Analog to Digital Converter (ADC) is the core and front end of digital systems, its residual noise has an important impact on the system performance. Consequently, the selection of the proper ADC becomes a critical issue for the system implementation. Currently, the information available in literature deeply describes the ADC features mainly at frequencies offsets far-from-carrier. Nevertheless for time and frequency applications the performance close to the carrier is an important concern as well. In this paper, a simple method for ADC characterization is proposed based on the Phase Locked Loop (PLL) definition and on Phase and Amplitude Modulation (PM/AM) measurements, focused in obtaining the relevant information of ADC noise contributions for phase noise measurement applications. The purpose of such a method is to find the parameters of a state ADC noise model using a technique which avoids the use of complex hardware and allows having a low computational costs performance.

Keywords—phase noise; analog to digital converter; digital signal processing; phase modulation; amplitude modulation; PLL

I. INTRODUCTION

Phase noise measurement has been an important subject of study due to the serial implications that phase noise has on systems in which high source frequency stability is required in order to guarantee a correct and accurate performance, such as radar applications, ultra-stable oscillators, data communication links and multichannel receivers.

Phase noise represents the random frequency fluctuations caused by phase instability [1]. Therefore, the phase noise measurement of a system source provides the information about its frequency stability. Since the phase noise is a critical parameter in the selection of the appropriated system source(s), different techniques have been developed in order to measure it, most of them based on the use of spectrum

analyzers and analog systems [2][3]. The classical phase measurement setup is the quadrature method depicted in Fig. 1.

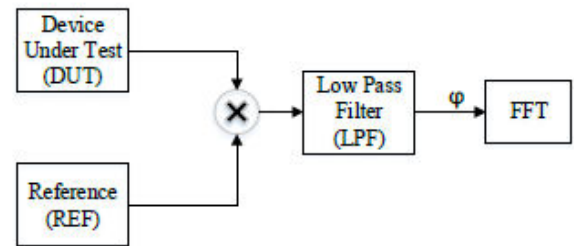


Fig. 1. Phase noise measurement. Quadrature method.

The measurement system works as an appropriate phase detector if the device under test (DUT) and the reference (REF) are in phase quadrature due to the mixer operating principle. Considering that meeting this requirement by manual configuration is not efficient neither easy, a feedback is added in order to keep the quadrature condition, as shown in Fig. 2.

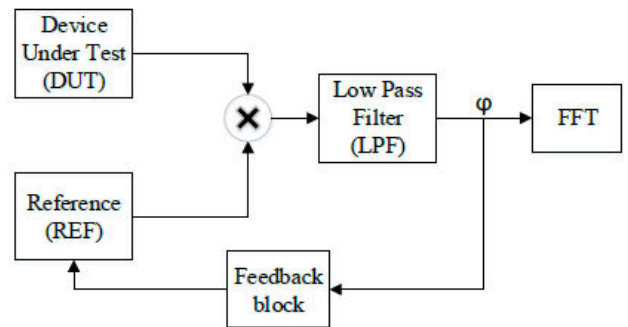


Fig. 2. Method with feedback to keep phase quadrature.

However, for a new DUT phase noise measurement, the feedback parameters must be adjusted depending of the DUT characteristics and the feedback typology implemented. It will imply to change hardware or recalibrate the measurement system which may become a time-consuming task.

Furthermore, considering that analog systems are highly affected by mechanical noise (50Hz – 1 kHz) and that most of the system characterization of interest works from mHz to tens of MHz offset with respect to the carrier, the phase noise measurement has to be performed under excellent conditions of mechanical noise isolation (hardware design - PCBs, connections between stages) increasing the complexity of the implementation.

The problems previously mentioned are not only evidenced in the quadrature method. Parameterization issue and mechanical noise are problems that affect in general analog systems. Hence, in order to increase the system flexibility and reduce the effects of mechanical noise, temperature dependence, drift, aging and tuning, approaches as Software Defined Radio (SDR) [4] has started to be applied.

In the ideal SDR concept, the system architecture will consist in an analog to digital converter (ADC) and in the digital process block (Fig. 3).

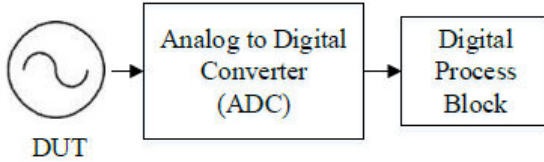


Fig. 3. Ideal SDR architecture.

However, due to technological limitations of ADC and signal processing bandwidth, the real SDR system architecture may differ from the ideal solution depending of the application requirements. For the case of phase noise measurement, the ADC bandwidth could be an important constraint to the system performance, therefore, in order to reduce the bandwidth of the ADC input signal, the mixing and filtering stages can be performed before sampling.

Nevertheless, the analog mixers introduce AM noise to the system, adding a contribution to the phase noise characteristics not related to the DUT and challenging to subtract from the records. Thus, considering that the recent technological advances allow finding ADC components with wide operational bandwidth in the market, the possibility to implement phase noise measurement systems as the ideal SDR concept states is feasible and has been applied with different techniques [5, 6].

But, how to know which ADC suites better or more properly phase noise measurement requirements?

Generally as first stage, the selection of an ADC is based on the datasheet information, in particular number of bits, sampling frequency, bandwidth and signal to noise ratio, features that determine the main characteristics of the measurement outcome. In time and frequency applications and in particular for phase noise measurements, the ADC noise

spectra provides additional information that allows the identification of ADC noise contributions to the data converted, and therefore the effects on the phase noise measured. Different techniques based on histograms and FFT analysis has been developed in order to characterize the ADC noise spectra [7]. Although such techniques are very useful for ADC characterization and test, they do not provide complete information about the ADC noise, due to the complexity of the hardware needed (components performances not still available, memory lack, etc.) especially at low frequencies, i.e., flicker noise, which may impact on phase noise measurements in oscillators at frequency offsets close-to-carrier.

Thus, the purpose of this work is proposed a method for ADC noise characterization that provides the ADC noise spectra at frequency from 1Hz or less using a simple system setup.

For accomplish this aim, a model of ADC noise is state, which sets the ADC noise as a function of two parameters or noise contributions, additive noise and jitter noise, as described in section II. Subsequently, based on this model, the method proposed will find such parameters through PM and AM measurements, tracking the relevant ADC information using a PLL (Section III). The implementation of this method was performed using Red Pitaya platform as explain in Section IV, which provides the hardware needed for a first approximation.

II. ADC NOISE MODEL DESCRIPTION

In order to discriminate the nature of the noise that can affect an oscillator signal, an ADC noise model was adopted (Fig. 4). It consists in three noise components. The first one, n_a , represents additive noise caused by thermal noise, circuit construction, voltage reference, which is presented mainly as amplitude modulation noise. The second one, n_j , represents the noise caused by the aperture jitter or aperture uncertainty in the sample and hold during the data acquisition, which is presented as phase modulation noise at the ADC output. The third component is the quantization noise, characteristic well known which is spread along the ADC bandwidth.

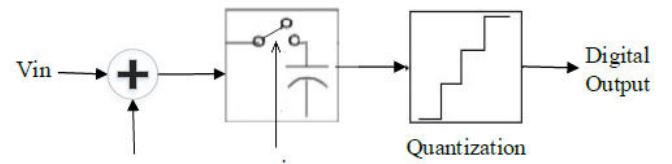


Fig. 4. ADC noise model adopted.

Hence, the model under study will depend only of the unknown components, being a function of the n_a and n_j parameters, as depicted by the eq. (1) that intrinsically will take into account the quatization noise effect.

$$n_{ADC} = f(n_a, n_j) \quad (1)$$

The main objective of using this model is to be able to predict the ADC noise contributors on the phase noise measurement based on the parameters information.

III. METHOD PROPOSED FOR ADC NOISE CHARACTERIZATION

According with the model described in the previous section, two parameters must be determinate, n_a and n_j , which generate amplitude and phase modulation noise respectively. From Fig. 5 can be observed how amplitude fluctuations affect the points of maximum amplitude in an oscillator while phase fluctuations are easily detected at the zeros-cross points. Thus, tracking these points of the ADC output, having as input a sinusoidal signal from an oscillator will allow determine the parameters value but including the noise of the oscillator as well.

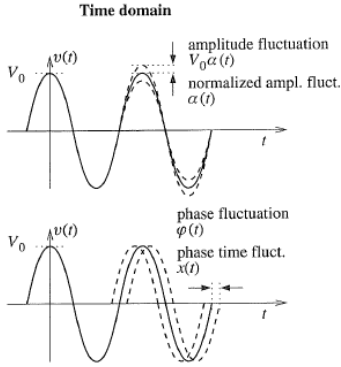


Fig. 5. Oscillator noise model. Amplitude and Phase Noise.

However, since the phase noise measurements under study are based on differential techniques, the digital instrumentation will used at least two independent ADC channels. Therefore, the ADC noise contribution to the phase-meter will be differential as well. In consequence, the common noise between the two ADC channels will be cancel and therefore the amplitude and phase fluctuations presented in the points mentioned above, will be traduced to ADC noise as described in Fig. 6.

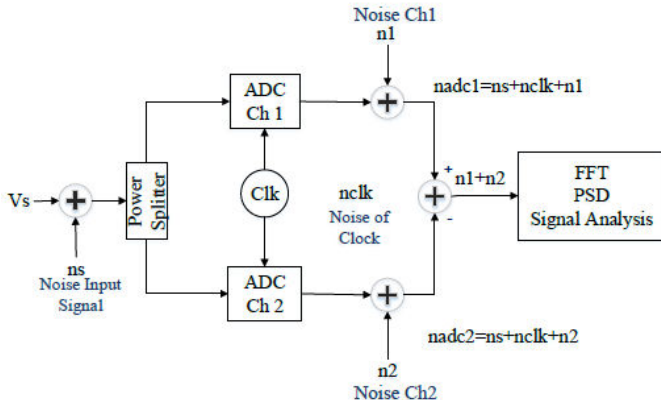


Fig. 6. Description of common noise cancellation using two ADC channels.

In order to track the points with relevant information of amplitude and phase fluctuations, the method depicted in Fig. 7 is proposed.

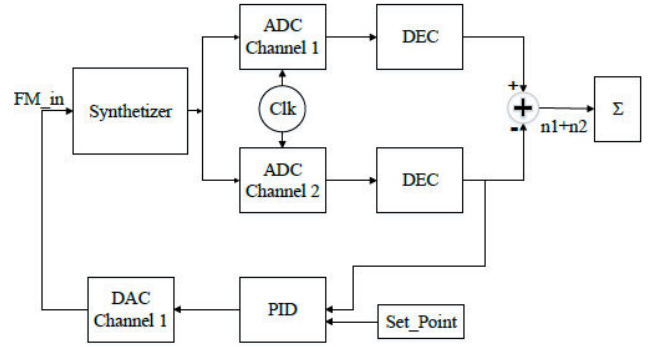


Fig. 7. Proposed method for ADC noise characterization.

The synthesizer will generate the sinusoidal input signal for both channels of the ADC, but one of them will be used also to track the points of interest using a down-sampling block (DEC) and a PI controller. The output of the controller will be connected to a DAC which will provide the proper information to the synthesizer that also works as Voltage Controller Oscillator (VCO) correcting the signal generated in order to acquire the set point configured, maximum amplitude point or zero-cross point.

The ADC noise spectra will be obtained performing the proper decimation and filtering. This last stage will consist in an accumulator and an average filter.

IV. METHOD IMPLEMENTATION

As platform for implementation or test bench was used Red Pitaya [9] an open source embedded system that includes a 14 bits ADC of two channels at 125MSps, a dual DAC of 14 bits at 125MSps and a System On Chip (SoC) Zynq 7010 from Xilinx (FPGA+ARM). Additionally, this platform counts with a PID controller block ready to be used and all the drivers for the ADC and DAC operation. Fig. 8 depicts the block diagram of the method implemented.

As input of the system, a sinusoidal input signal was generated with carrier frequency (v_0) of 31.25MHz and 1.5Vpp. Due to the fact that the input frequency is four times the sampling frequency (125MHz), the down-sampling factor is set to four. With this configuration is acquired one sample per period, which can be the maximum amplitude point or zero-crossing point, depending of the system configuration. The data are store in memory blocks of 16384 samples each one of 32bits, i.e., blocks of around 65Kbytes.

The PID controller actually is a controller Proportional and Integral proper configured to track the points of relevant noise information.

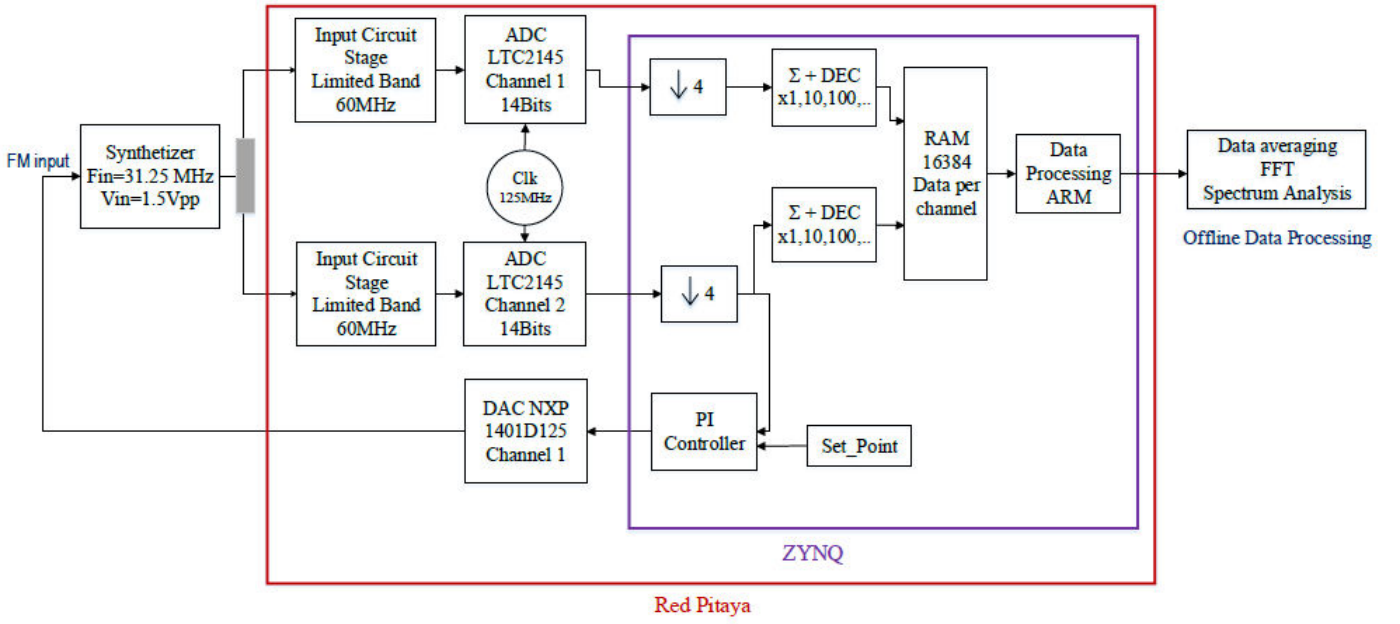


Fig. 8. Description of the implementation of the proposed method for ADC noise characterization

V. RESULTS

A. PM measurement approach – n_{jitter} parameter

In Fig. 9 is shown the noise spectra of the component n_j measured using an input signal of $v_o=31.25\text{MHz}$ (blue curve). The pink spectra is the same component measured without input, i.e., with a load resistor of 50Ω .

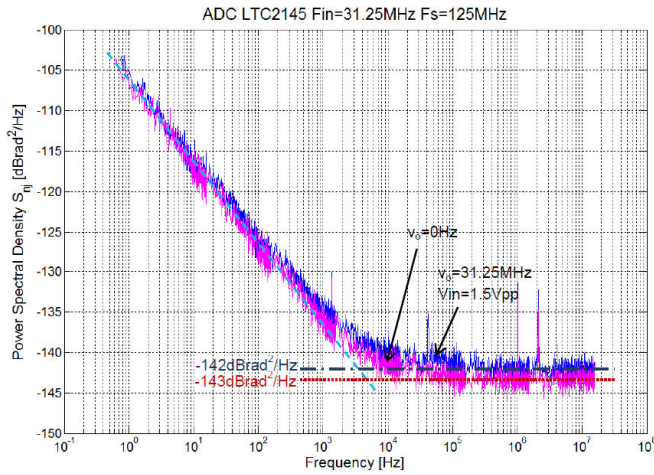


Fig. 9. Spectra of jitter noise contribution on ADC noise through PM measurements. Slope of $-10\text{dBrad}^2/\text{Hz}$ cyan dot line (Flicker noise)

It can be observed how the jitter effect start to be evident increasing the white noise of the spectra when the frequency of the input signal increase, as was expected, due to the fact that the slope of the signal acquired increase being more sensitive to these phase fluctuations. The noise a low

frequencies has a slope of $-10\text{dB}/\text{Hz}$ than means flicker noise, which remains with the same value.

B. AM approach – additive noise parameter

Fig. 10 depicts the spectra of the additive noise component, n_a referred to the spectra measured without input signal. In this case the white noise did not change because whether the amplitude fluctuations is low it will not affect the ADC spectra.

It can be observe noise around 80KHz that could be caused by the internal reference of the ADC whose effect was not cancel due to the fact that this is an ADC noise source that must be considered.

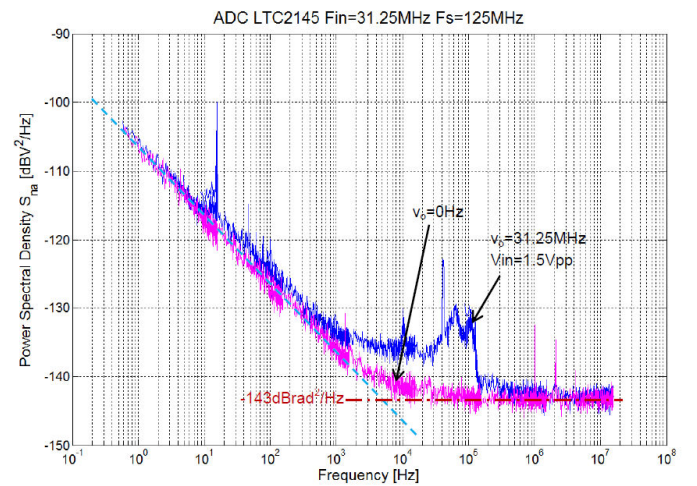


Fig. 10. Spectra of additive noise contribution on ADC noise based on AM measurements. Slope of $-10\text{dBrad}^2/\text{Hz}$ cyan dot line (Flicker noise)

The white noise in both figures presented above does not take into account the aliasing contributions caused by the down-sampling process. Since it is the sampling frequency is divided by a factor of 4, the white noise is reduced 6dB.

The table reported below, depicts preliminary results about the ADC noise parameters. This first approximation can be compared with the performance of a generic analog mixer which has a flicker noise around -140dBrad²/Hz at 1Hz [10].

TABLE I. ADC NOISE MODEL PARAMETERS

<i>Parameter</i>	<i>White Noise</i>	<i>Flicker Noise</i>
n_a	-149 dBV ² /Hz	-106 dBV ² /Hz
n_{jitter}	-148 dBrad ² /Hz	-105 dBrad ² /Hz

VI. CONCLUSIONS

Preliminary results were obtained for the ADC noise parameters. It is imperative to validate the method under different conditions, using different ADC architectures and technologies in order to verify the accuracy of the method.

The measurements performed provide information along seven decades using approximately 40% of the FPGA resources, which implies not high computational resources.

The spectra obtained present low spurious along the bandwidth, it means not excess of noise caused by the digital processing.

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