Noise in High-Speed Digital-to-Analog Converters

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***Abstract*—We report on the measurement of phase noise of high speed analog to digital converters in a full digital measurement setup and for various development boards. The tested configurations ensures a Nyquist rate higher than 100 MHz suitable for conventional ultralow noise devices. Several analog to digital converters presenting a SNR higher than 140 dB enable mesurement floors of around -185 dBc and below -160 dBc off the carrier using cross-correlation technique.**

I. Introduction

Digital tools are a mature technology to perform dynamic signal analysis on ultrastable clocks and devices presenting unpreceedent levels of stability[1-3]. Jointly with the help of Soc FPGAs used as realtime coprocessors and CPUs running multitasks operating systems with double precision, cross-correlation techniques on full samples phase times series benefit from high bandwidths up to 100 MHz off the carrier. The IF conversion is done after sampling, analysis resolution is limited in the measurement time by the resolution of the analog to digital converters. We present in this paper various tests performed on several kind of platforms based on FPGAs with deported CPUs or the latest SoCs embedding hard cores CPUs.

II. Numbers

Assuming a uniform quantizer, the quantum resolution step is defined as the ratio of the voltage full scale range and the number of bits M:

$$q = \frac{v_{fsr}}{2^M - 1} \tag{1}$$

The associated noise is a statistical process representing the density of probability of states within a measurement lenght τ :

$$\sigma^2 = \frac{1}{\tau}\int_{-\tau/2}^{\tau/2} e_q^2(t)\mathrm{d}t = \frac{q}{12} \tag{2}$$

Finally the total noise represents the integrated noise over the measurement bandwidth, directly related to the Nyquist frequency :

$$\mathcal{N} = \frac{\sigma^2}{f_N} \tag{3}$$

This last equation remains only when proper filtering and small fraction of aliasing occurs, thanks to Parseval theorem.

Eventually, for an incoming wave of peak voltage $a \sim v_{fsr}$, one may derive the signal to noise ratio :

$$SNR = \frac{4 \cdot q^2}{3 \cdot v_{fsr}^2 \cdot a^2 \cdot f_s} \sim \frac{4}{3 \cdot 2^M \cdot f_s} \tag{4}$$

where f_s represents the sampling rate.

III. Digital Architectures

In this project, we have operated a selection of various platforms with integration of FPGA and CPU cores. All algorithms have been developped from scratch in C as a library featuring basic blocks functions, double and single precision in order to predict correct behaviour of their hardware description counterparts. To our point of view, this is the correct way to fully master the full system flow and measurement chain at every stage. In this manner it will be possible in the future to develop accurate models including quantization noises processes. Indeed this excludes the use of any proprietary black-boxes.

We present here 3 digital architectures that are, amongst others, under test at FEMTO-ST.

We have selected a high-speed digitizing system, from Alazartech company, consisting of 2 synchronized boards embedding each 2 AD9467 (16 bits, 250 Msps), 2 Altera Stratix III FPGAs (main/coprocessor) and PCIe extension connected to multicore PC station running debian-based GNU-Linux kernel 3.16. The versatility of such a system enable ease of retrieving continuous samples at full speed, fast developpment and algorithms testing as the interfaces and communication parts are already provided.

Second, the recent multicore SoC FPGAs as Zynq/Cyclone V systems offer potential high-end features and are of growing interrest. For we have conducted tests on Zynq-based platforms (ZC706 coupled to 2 dual-channel LTC2158 (14 bits, 310 Msps), and also tested the dual-channel LTC2145 (14 bits, 125 Msps) of the Redpitaya system, although this last platform is more dedicated to low-quality general purposes (small FPGA, only 2 channels, not Open Source/Hardware…).

IV. Phase noise measurement setup

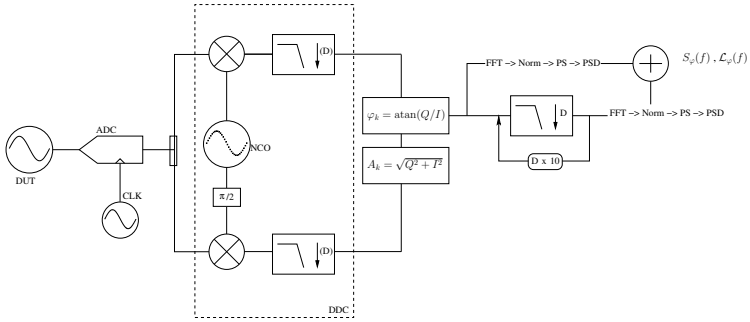


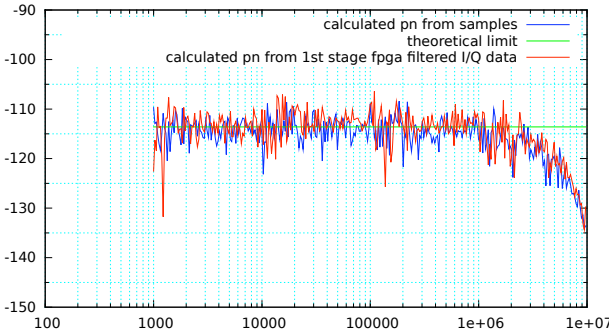
Fig. 1. Principle of a digital phase noise measurement system

The digital phase noise measurement system[3] is depicted in the preceeding figure. The phase modulated noise degrading

a perfect sinusoid is downconverted to DC after sampling thanks to a numerically controlled oscillator (NCO) set up at the carrier frequency. Successive filtering/decimation stages allows to focus on lower decades off the carrier or examine the spectral measure at lower sampling rates by filtering out aliased noise while reducing the measurement bandwidth. Phase estimation is done by calculating the arctangent function of the in-phase and quadrature components of the demodulated and filtered signal. Eventually the amplitude is also estimated. From the phase time series (amplitude time series), the Fourier transform is computed thanks to the FFTW[4] algorithm. Other filtering/decimation stages completes the process of lowering the decades. Finally the spectrum of variances is reconstructed from these decades. The demodulation process and first decimation/filtering stages may be abusively called digital down converter (DDC).

V. Software calibration

In order to verify the correct interpretation of the spectral measure (normalizations processes), a noise generator calibrated at -113 dBc mixed with a low noise 10 MHz reference signal is send to the analog to digital converter.

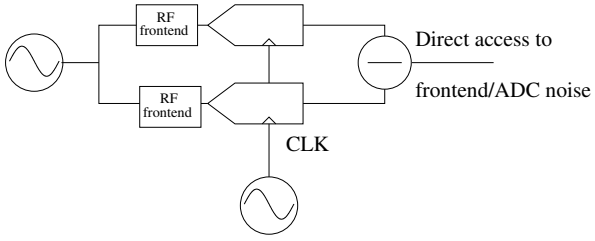


The power spectral density is evaluated from the collected samples at full speed with double precision (*'calculated pn from samples'* in the figure). The counterpart digital down conversion in single precision version embedded into the FPGA, by using a squarewave NCO (inverted samples every 25 points per period for a 10 MHz carrier at 250 MHz sampling rate) and a 127 coefficients Blackman-Harris windowed sinc filter to ensure sufficient aliased noise rejection, shows similar results. The first stage output effectively ensures that no extra quantization noise is induced by the chain, particularly the full bit width remains unchanged. This process is no longer true when multiple stages must be embedded while performing slice rescaling, and additive noise may be taken into account.

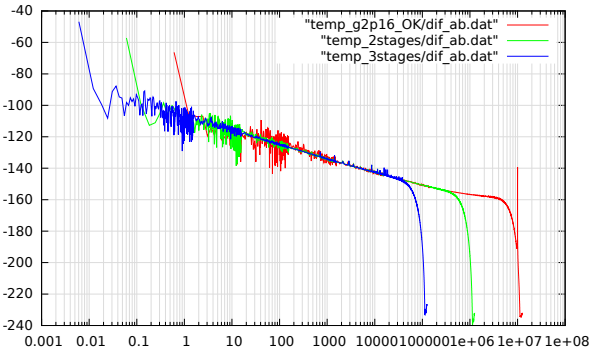
VI. ADC noise measurements

A. ADC noise measurement principle

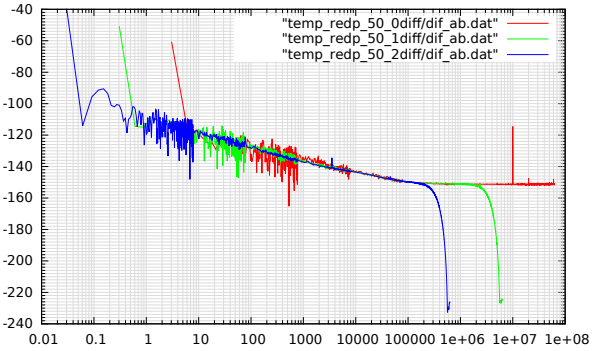
The setup of ADC phase noise measurement is depicted in the following figure.



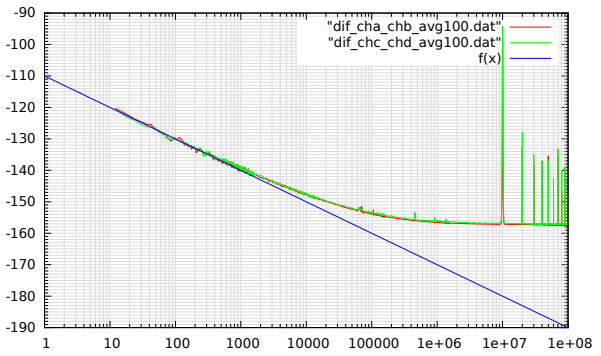
A splitted low noise 10 MHz synthesizer feeds the rf-frontend and ADC. Both arms are differentiated, allowing the common clock noise circuitry to be inherently filtered out. Only remains a small fraction. The differenciation allows a direct interpretation of the noise of the frontend/ADC couple. Unless specified, the clocking system was done with an external low-noise synthesizer. Successive filtering/decimation processes (up to 3 embedded into the FPGA) enable a fast estimation of the system noise. The sinc filters are based on Kaiser window with 128 convolutions. Careful adjustment of gains and rescaling ensure the lowest added quantization noise. The resulting voltage noise spectrums are shown in the following figures for the 3 tested ADCs ($\mathrm{dBV}^2/\mathrm{Hz}$).



For the LTC2158, the input carrier was 6.6 dBm, with a voltage fullscale range of $v_{fsr} = 1.35$ V. Slices of 2^{17} points were taken at every output stage of the filters to reconstruct the spectrum. White noise is about 10 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and flicker of 5.6 $\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$. SNR=154 dB for white noise.



For the Redpitaya system, the input stage was bypassed and loaded to 50 Ω. Only the LVDS amplifier was kept to prepare the ADC to be feeded with differential signal. The gain is about 2, for a 0 dBm signal and a $v_{fsr} = 1.25$ V at the input of the analog to digital converter (the measure was done in a differential mode). The onboard clock system was used to clock the ADC at 125 Msps, slices of 2^{14} data were taken, and because of spare space, only two filtering/decimation stages were performed within the FPGA. The obtained white noise is $29\mathrm{nV}/\sqrt{\mathrm{Hz}}$, and $4.5\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$ for flicker. SNR=143.5 dB (white) in a 1Hz bandwidth.



Results from the AD9467 of the Alazartech boards presented, for a 12 dBm carrier ($v_{fsr} = 2.5$ V), a white noise floor of about -157 $\mathrm{dBV^2/Hz}$ (14 $\mathrm{nV/\sqrt{Hz}}$) and a flicker of $-110\mathrm{dBV^2/Hz}$ (3 $\mu\mathrm{V/\sqrt{Hz}}$). Referred to the carrier, this is equivalent to a SNR of 156 dB (white) and 109 (1 Hz) in a 1 Hz bandwidth.

Taking into account the 1 dBc of carrier power, the presented results are compatible with phase noise measurements.

B. Effective number of bits evaluation

This technique is perfectly suitable to a fast evaluation of the effective number of bits (ENOB) of the analog to digital converters. One may just analyze the white noise floor for quick evaluation of the ENOB. Technically, this may only need 1024 samples for example and a FFT evaluation on 512 points, or even less ; to get better accuracy, simple averaging may help. We have derived the ENOB calculation assuming uniform quantization and the fact that it is directly related to the signal to noise ratio :

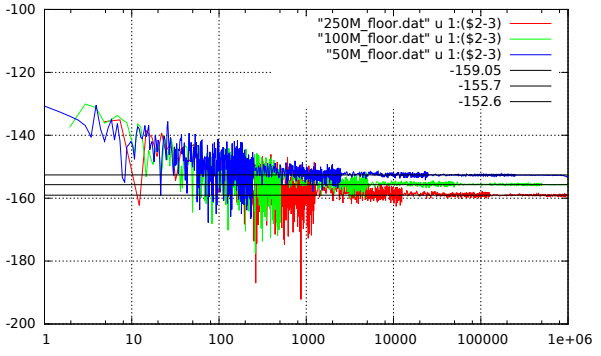
$$ENOB = \log_2\left(1 + \frac{v_{fsr}}{\sqrt{12 \cdot f_N \cdot S_{floor_L}}}\right) \qquad (5)$$

where S_{floor_L} is the measured white voltage noise floor, v_{fsr} is the voltage full scale range and f_N the Nyquist frequency.

Applied to the AD9467 system, the measurement of $S_{floor} \sim= -158$ $\mathrm{dBV^2/Hz}$ lead to an effective number of bits of about 12 in agreement with the technical datasheet.

C. ADC noise vs sampling rate

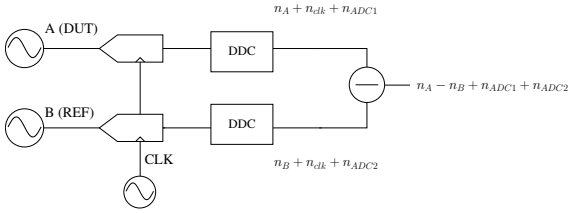
White phase noise floor directly depends on the sampling rate as shown on the following figure.



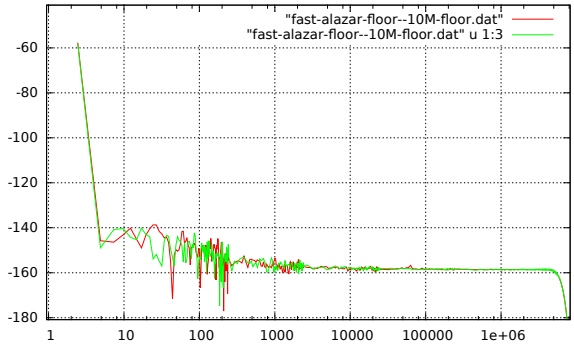
The measured noise floors for various sampling rates are in perfect agreement with their theroretical expectations.

VII. Single channel noise measurement

The digital single channel noise floor measurement obeys the setup described on the following figure. When the two converters are feeded with a full scale range 10 MHz low noise wave, we may have access to the single channel noise by differentiating the 2 arms after digital down conversion, phase extraction and spectrum calculation.



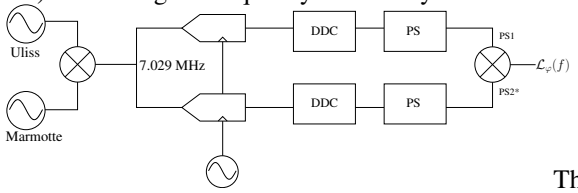
For the noise budget, the uncorrelated arms noises are suppressed and just remains the contribution of the converters noises.



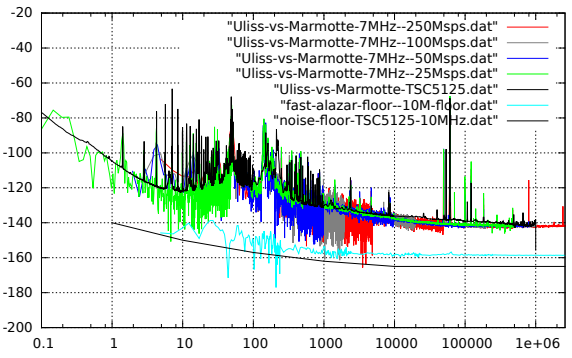
The presented $\mathcal{L}_f$ spectrum shows it is possible to perform measurement of low noise oscillators up to -160 dBc without the need of more complex architecture.

VIII. Application to the measurement of CSO

It is possible to apply the 2 channels technique to the measurement of a pair of cryogenic sapphire oscillators (CSO) exhibiting a frequency instability in the 10^{-15} range.



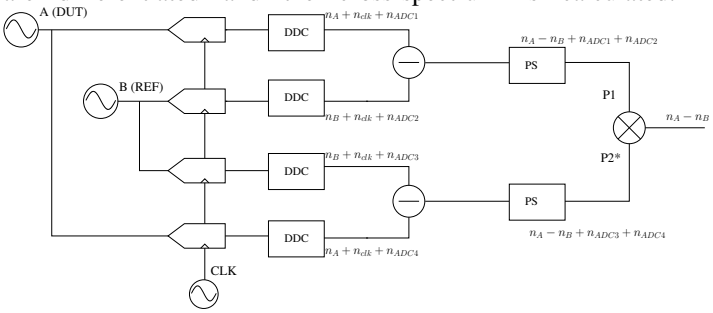
The beatnote of about 7.029 MHz of a pair of CSO feeds a two-channel digital phase noise measurement system. The beatnote is downconverted and successive filtering/decimation stages are applied.



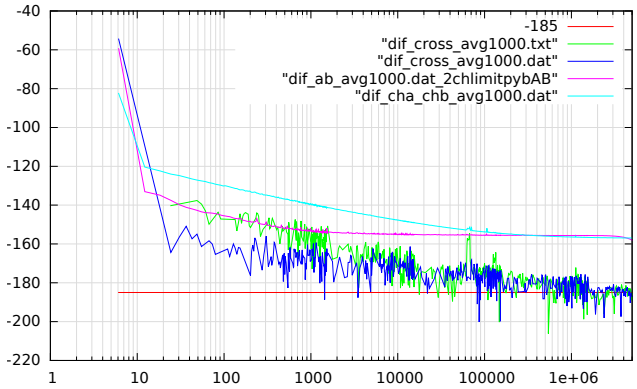
The setup favorably compares with the indicated noise floor of the TSC5125 but with only a 2 channels configuration.

IX. 4-CHANNELS DIGITAL SIGNAL ANALYZER WITH CROSS-CORRELATION

We have applied the all-digital 4-channel cross-correlation technique as described in [3]. After sampling and gain adjustment, the digital down conversion is applied and phase extracted from the I/Q data flow at a rate of 25 Msps. The phases time series of 2 pairs of channels are differentiated and the cross-spectrum is calculated.

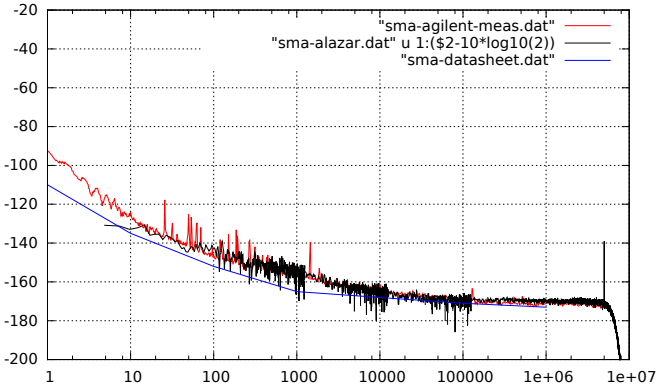


For the measurement of the system noise floor, a 10 MHz signal is send to each of the 4 channels. With 10^7 correlations on a continuous data flow, the obtained floor quickly reaches -185 dBc and is below -160 dBc for Fourier frequencies at 10 Hz off the carrier (1000 correlations).



Better results could be expected, even if they already represent state-of-the-art results.

As an application, we have performed the measurement of the low noise synthesizer used in our experiments, the R&S SMA 100A with low noise option. The resulting plot is compared to the expensive Agilent PN5052B.



X. CONCLUSION

In this paper we have presented a correct all-digital technique for the evaluation of the noise of high-speed analog to digital converters. The setup is suitable for fast analysis of the effective number of bits of such converters, the main parameter related to quantization noise and signal to noise ratio, directly impacting the resolution of digital measurement systems. A 2 channel phase and amplitude noise measurement system has been developped and applied to the measurement of ultra-stable cryogenic sapphire oscillator. Also we have presented an extension of a 4-channels cross-correlation system resulting of noise floor of -185dBc, confirming the potential of such a technique.

ACKNOWLEDGMENT

This work was supported by the PIA Oscillator-IMP platform and by the Nihon University, Japan.

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[4] http://fftw.org/ ; FFTW was written by Matteo Frigo and Steven G. Johnson