

Sub-picosecond Software Defined Radio receiver synchronization for multi-radiofrequency band time and frequency transfer

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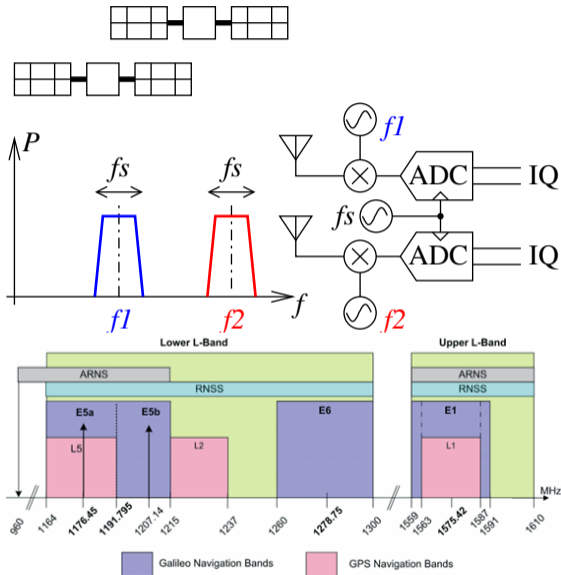
Context

- ▶ Distributed radiofrequency signal acquisition system...
- ▶ ... spanning multiple frequency bands (E1, E5, E6)...
- ▶ ... collecting samples for post-processing.
- ▶ Each SDR receiver can only sample up to individual L-band bandwidth

⇒ how to synchronize multiple SDR receivers and make sure the synchronization is stable upon cold-start of the system

⇒ delay calibration

Objective: sub-100 ps stability and reproducibility



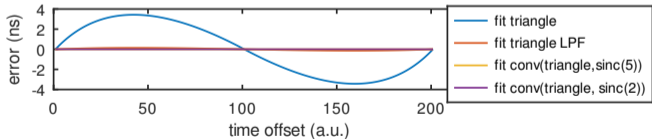
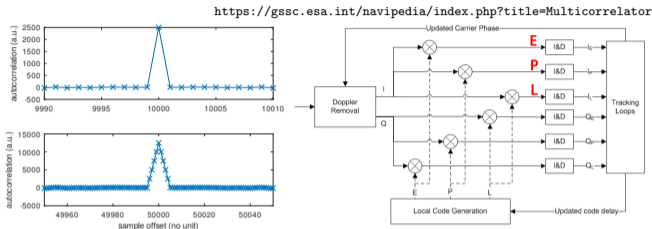
Background

- ▶ Sampling a Pseudo-Random Number (PRN) sequence generated at f_N chips/s at a rate of f_s samples/s leads to a cross-correlation peak with f_s/f_N samples (autocorrelation function)
- ▶ Parabolic fit of this correlation peak allows for sub-sampling period resolution
- ▶ Timing improvement given by

$$dt = \frac{T_s}{2} \frac{y_{-1} - y_1}{y_1 + y_{-1} - 2y_0}$$

with y_k the cross correlation peak magnitude ($k = 0$ at maximum, $k = \pm 1$ neighbours)

- ▶ dt fluctuation determined by y SNR
- ▶ $f_s = 1/T_s$ limited by communication/storage bandwidth, allocated channel/signal bandwidth
- ▶ in these experiments, $f_s = 5$ MS/s matching a 2.5 Mchips/s BPSK PRN $\Rightarrow T_s = 200$ ns
- ▶ sub-100 ps: **2000-fold** improvement on timing capability \Rightarrow need for such an SNR on reference pattern



Issue with fitting a triangle with a parabola... oversample & low-pass filter, or zero-padding

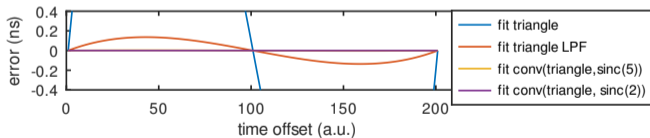
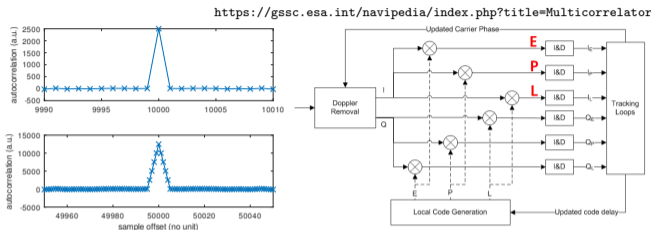
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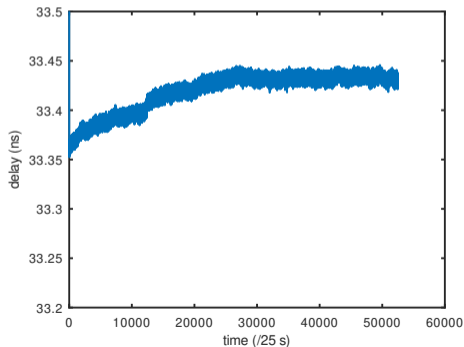
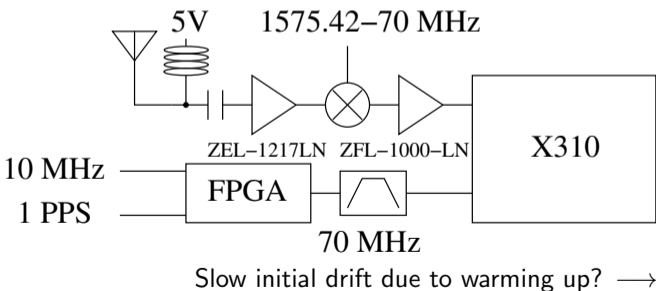
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Time distribution to multiple SDR receivers

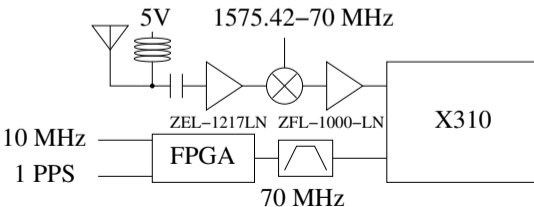
- ▶ Use Ettus Research X310 SDR receivers with BasicRX (balun→ADC) and external mixer/amplifiers/filters
- ▶ A local pseudo-random code generator at 70 MHz IF frequency feeds a reference channel while the second X310 channel records the GNSS signal offset by 70 MHz
- ▶ Record IQ complex stream at 16 bit/sample on both channels: $5 \cdot 10^6 \times 2 \times 2 \times 2 \times = 40 \text{ MB/s}$ or 72 GB in 30 min
- ▶ **post-process** binary file with gnss-sdr (v.0.0.19) to extract Obs and Nav files



Time distribution to multiple SDR receivers

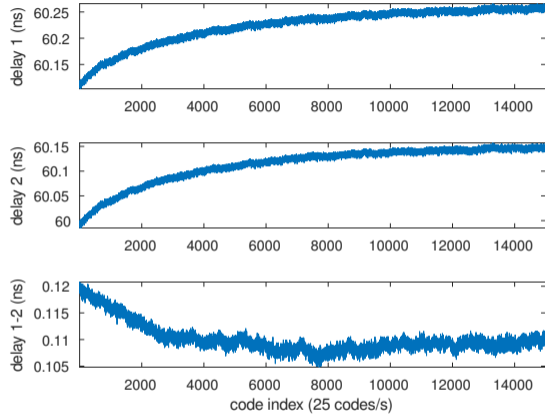
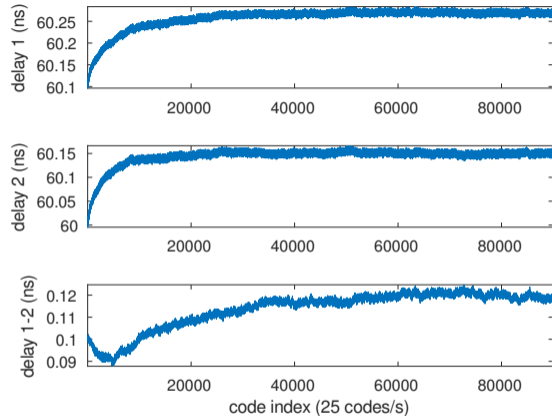
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- ▶ **post-process** binary file with gnss-sdr to extract Obs and Nav files: not a single sample was lost during the acquisition

```
[...]
PVT.implementation=RTLILIB_PVT
PVT.averaging_depth=100
PVT.flag_averaging=true
PVT.output_rate_ms=10
PVT.display_rate_ms=500
PVT.rinex_output_enabled=true
PVT.rinex_name=Lloutput.rinex
PVT.rinex_version=2
```



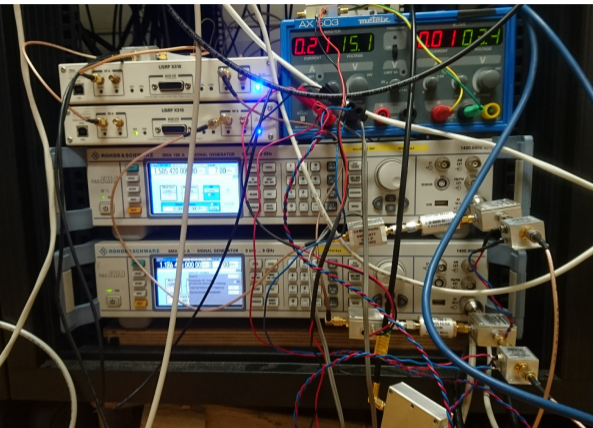
GNSS-SDR		Software Receiver					0.0.17		REC # / TYPE / VERS		
Antenna number		Antenna type							ANT # / TYPE		
0.0000		0.0000				0.0000		APPROX POSITION XYZ			
0.0000		0.0000				0.0000		ANTENNA: DELTA H/E/N			
1	1								WAVELENGTH FACT L1/2		
4	C1	L1	D1	S1						# / TYPES OF OBSERV	
2023	07	03	16	41	18.1200000	GPS		TIME OF FIRST OBS			
18									LEAP SECONDS		
										END OF HEADER	
23	7	3	16	41	19.0000000	0	7G31G03G06G07G09G19G17				
24869208.870		7	130688727.094		7	-2705.793		7	42.623		
22986458.350		7	120794809.325		7	-2529.179		7	47.237		
21569158.442		8	113346845.827		8	1077.469		8	49.424		
24866463.438		7	130674300.985		7	3315.916		7	43.655		
21205949.822		8	111438170.255		8	1028.520		8	50.955		
23840192.164		7	125281192.873		7	-2811.177		7	42.801		
24808318.700		6	130368747.427		6	-2992.182		6	40.965		
23	7	3	16	41	20.0000000	0	7G31G03G06G07G09G19G17				
24869687.188		7	130691436.080		7	-2707.835		7	42.298		
22986907.577		7	120797338.529		7	-2529.456		7	47.711		
21568920.900		8	113345768.035		8	1076.706		8	48.889		
24865803.195		7	130670985.692		7	3316.947		7	43.544		
21205722.233		8	111437141.290		8	1028.817		8	51.250		
23840691.558		7	125284003.446		7	-2812.247		7	42.400		
24808853.672		6	130371737.899		6	-2989.092		6	40.670		

Warmup drift (1 h and 10 min records)



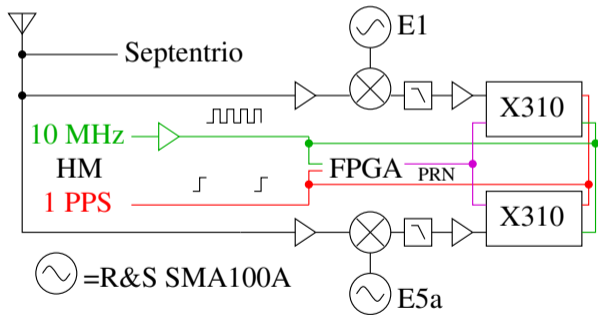
- ▶ Same drift observed on both X310s (2 successive experiments) so that the difference is in the < 100 ps range
- ▶ Stationary steady state if the ADCs keep on running and streaming data (ZeroMQ) which are only collected when needed (not further explored here)
- ▶ Cables were **swapped** between left and right experiment (assess reproducibility of delay between X310s)

Duplicate to as many radiofrequency bands as targeted



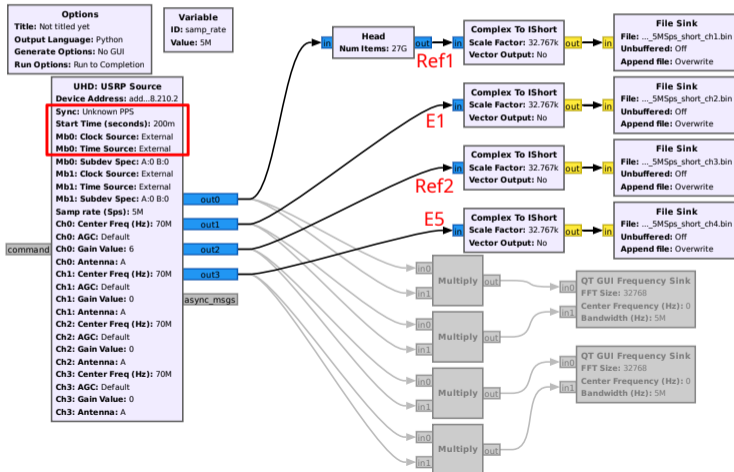
All reference signals are provided by the Besançon Time & Frequency (LTFB) hydrogen masers

- ▶ Single GNSS antenna split to multiple receivers (active splitter between SDR and Septentrio)
- ▶ Fast comparator converts 10 MHz sine wave to square wave for clocking the FPGA



Results with synchronized acquisition + E1 + E5: impact of f_s

- ▶ Synchronization: 70 MHz IF with 2.5 Mchips/s BPSK PRN sequence to both X310 channel A
- ▶ E5a: 1176.45-70 MHz to X310 (1) channel B
- ▶ E1: 1575.42-70 MHz to X310 (1) channel B



- ▶ gnss-sdr generates 30 s RINEX output
- ▶ use github.com/georust/rinex for subtracting pseudo-ranges, requires the same header to match observations \Rightarrow **update** headers to match entries
- ▶ sampling frequency f_s derived from input 10 MHz, must be an **integer fraction** of 200 MHz

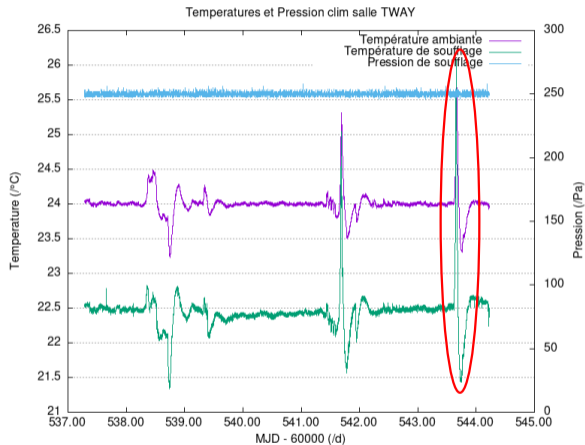
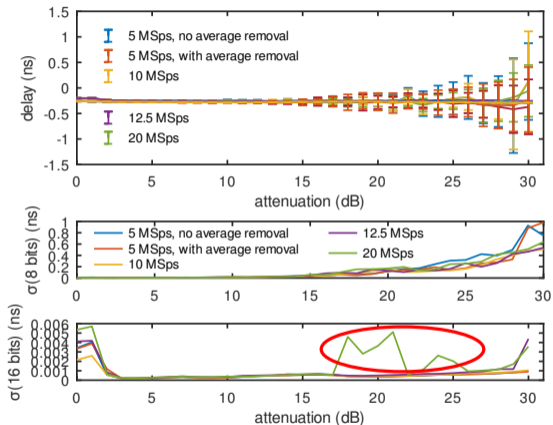
Results: Septentrio-gnss-sdr (ns) pseudo-range difference as a function of **sampling frequency f_s**

sampling freq. f_s	σ_{L1}	σ_{E1}	σ_{E5}
5 MHz	23.60	16.45	13.26
10 MHz	19.71	13.83	12.67
12.5 MHz	16.68	19.31	15.02

possibly limited by the positioning capability of gnss-sdr (no fixed-receiver solution with time only)

Impact of ADC resolution on SDR synchronization

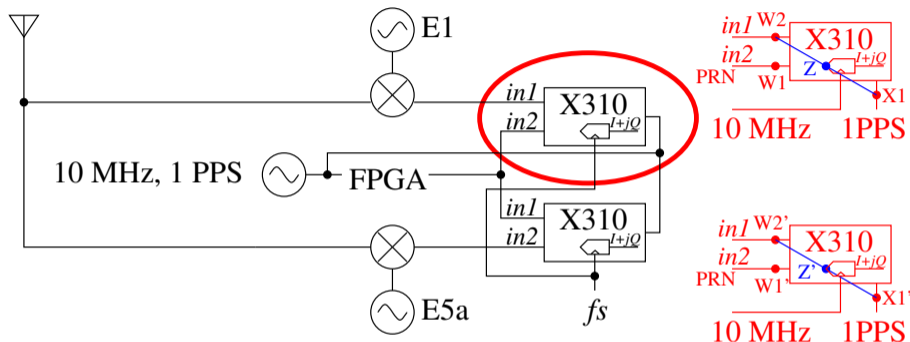
X310s running continuously to avoid warmup issue



Huge impact of temperature (red ellipses)

Need to keep **all 14 bits** for best PRN timing capability (time resolution improvement = synchronization signal SNR)

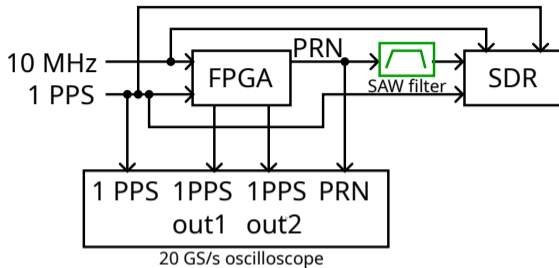
Delay to latching point Z



- ▶ Internal delay between latching point Z and the 1 PPS reference input X considering the PRN delay $W1$ has been verified to match measurement input $W2$.
- ▶ 10 MHz clock distribution cable length directly observed on delay (phase of SDR clock wrt PRN FPGA clock) \Rightarrow requires tight control of all clock distribution cable lengths

Estimation of 1-PPS delays

- ▶ 1-PPS used as external SDR trigger source
- ▶ 1-PPS used as FPGA trigger source (starts broadcasting PRN code when enable is high and rising edge of 1-PPS)
- ▶ ADC acquisition at 10 MS/s on both channels with 70 MHz frequency transposition (NCO + DDC)
- ▶ Two 1-PPS generated by FPGA:
 - ▶ 1-PPS out1 is input 1-PPS propagating through the FPGA gates
 - ▶ 1-PPS out2 is generated by a counter clocked by the internal FPGA PLL also clocking the PRN code generation
- ▶ SDR Channel 1 = PRN code ; channel 2 = 1-PPS input (high-pass coupled through BasicRX balun)



The SAW filter (green) is the source of a $2.35 \mu\text{s}$ delay (see datasheet):



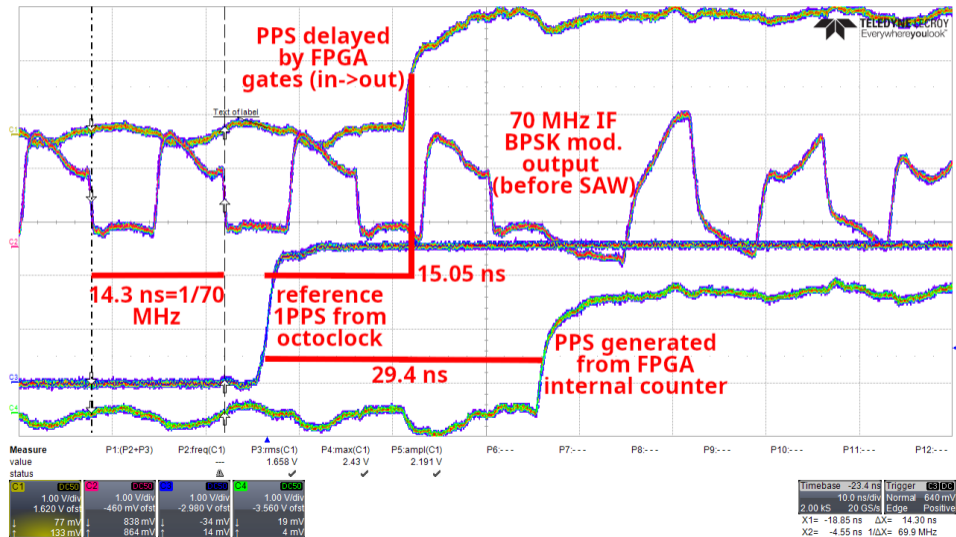
Data Sheet

70 MHz Bandpass Filter
2.5 MHz Bandwidth
Part Number 851547

Specifications				
Parameter	Unit	Minimum	Typical	Maximum
Center Frequency	MHz	69.92	70	70.08
Insertion Loss at f_0	dB	-	25.2	27
1 dB Bandwidth	MHz	2.1	2.25	-
3 dB Bandwidth	MHz	2.5	2.6	-
40 dB Bandwidth	MHz	-	4.12	4.4
Passband Variation	dB	-	0.28	0.7
Phase Linearity	deg	-	2	4
Group Delay Variation	nsec	-	45	100
Absolute Delay	μsec	-	2.3	-
Ultimate Rejection	dB	50	60	-
Substrate Material	-	-	Quartz	-

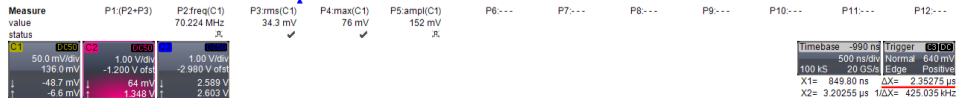
1-PPS measurement on FPGA transmitter

Input 1-PPS (from Octoclock) v.s 1-PPS running through the FPGA v.s 1-PPS generated by counter clocked by internal PLL



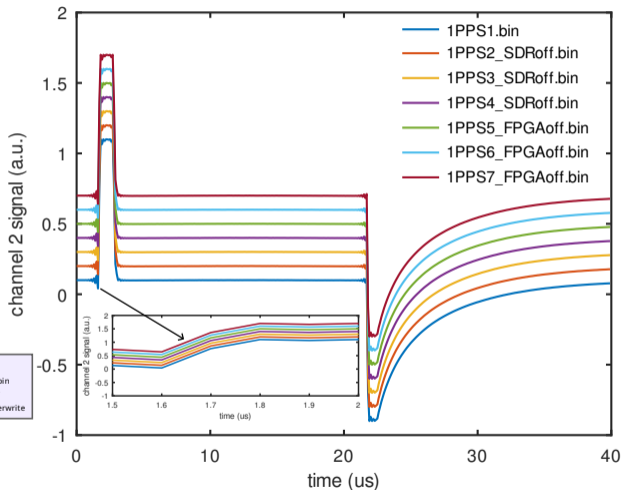
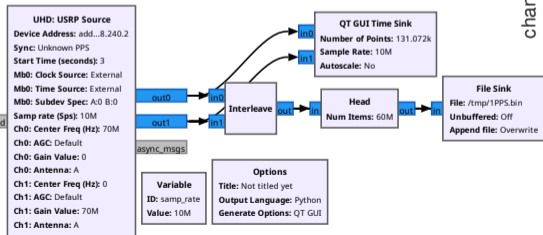
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ADC delay + reproducibility tests

- ▶ FPGA and X310 verified to align to reference 10 MHz and 1-PPS at each cold-start (select External Clock Source and External Time Source)
- ▶ Coarse analysis: feed RF input measurement channel with 1 PPS
- ▶ Fine analysis: cross-correlation of PRN reproducibility to ± 20 ps from one start to another

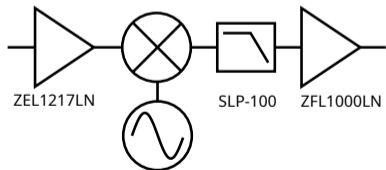


GNSS microwave reception chain delay (VNA delay measurement)

RF downconversion chain delay calibration τ_g using group delay from VNA $\varphi(f)$ measurement

$$\varphi = 2\pi f\tau \Rightarrow \tau_g = -\frac{1}{2\pi} \cdot \frac{d\varphi(S_{21}(f))}{df}$$

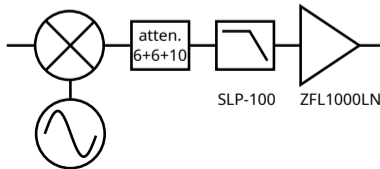
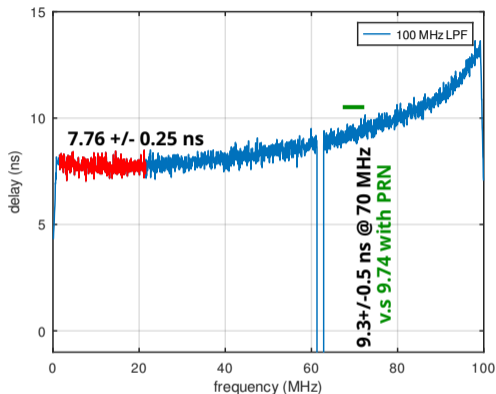
- ▶ VNA can only analyze linear components (cables, attenuators, filters, amplifiers)
- ▶ Rohde & Schwarz ZNB-8 Vector Network Analyzer, 50 MHz bandwidth, 2001 points, 1 kHz IF bandwidth, ∞ averaging
- ▶ 6+6+10 dB attenuators: 0.6₃ ns delay
- ▶ SLP-100 low pass filter: 9.6₇ ns delay
- ▶ ZFL-1000LN amplifier: 0.6₃ ns @ 70 MHz
- ▶ ZEL-1217LN amplifier: 0.8₃ ns @ 1575 MHz
- ▶ ZEL-1217LN amplifier: 0.9₆ ns @ 1175 MHz



Measurement at ± 100 ps at best \Rightarrow use PRN for fine delay analysis

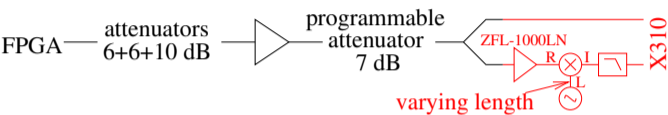
GNSS microwave reception chain delay (PRN + X310 measurement)

- ▶ FPGA + SAW low-pass + attenuator **common** to both reference and measurement channels until splitter, PRN carried on 70 MHz carrier
- ▶ One reference arm remains **unchanged**, one measurement arm incrementally filled with components
- ▶ equal length cable from splitter to inputs: 13 ± 2 ps
- ▶ attenuators only (to avoid saturation with ZFL100): 560 ± 2 ps
- ▶ attenuators + ZFL1000LN amplifier: 1082 ± 4 ps
- ▶ attenuators + SLP100 LPF + ZFL1000LN amplifier: 10817 ± 4 ps
- ▶ measurements consistent for linear components with VNA measurements, e.g. 100 MHz LPF
VNA method: 9.3 ± 0.5 ns (varying delay region)
PRN method: 9.74 ns delay around 70 ± 2.5 MHz
- ▶ mixer LO input oscillator set to **140 MHz** so that mixing with PRN at 70 MHz outputs 70 MHz

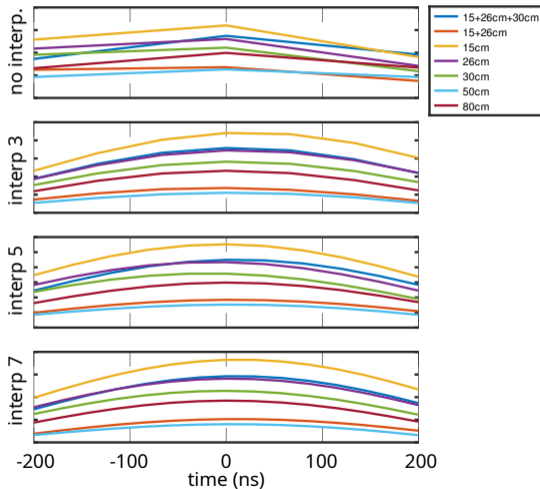


Mixer delay dependence with LO input phase using PRN method

- Baseline = FPGA + 6+6+10 dB attenuation + ZX60-100VHX amplifier + programmable attenuator (7 dB) + splitter

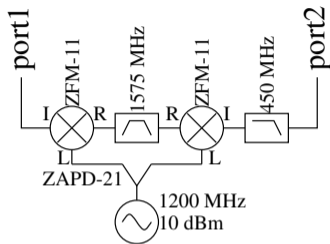


Experiment	delay (ps)
Baseline	6.2
ZFL-1000LN	780
ZFL-1000LN + SLP-100 LPF	10584
ZFL-1000LN + mixer + SLP-100 LPF	10150
add 16 cm to mixer RF input	20960
add 27 cm to mixer RF input	28060
add 43 cm to mixer RF input	38760
add 50 cm to mixer RF input	45825
add 150 cm to mixer RF input	9640

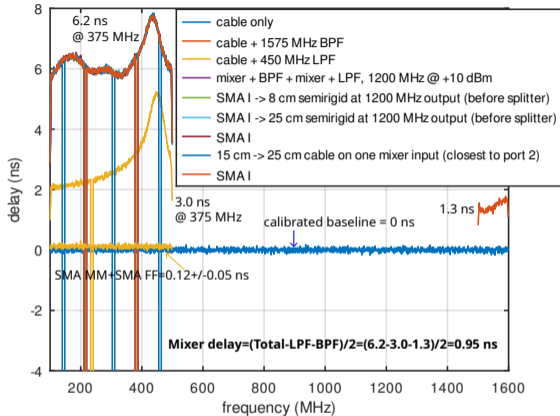


Result unexplained

Mixer delay using VNA¹²³



- ▶ **Assumption:** two mixers must exhibit the same delay (“golden mixer”)
- ▶ Group delay measurement: **0.85 ± 0.1 ns**
- ▶ ... verified to be independent on LO or RF frequency



¹P. Sarson & al., *Group delay measurement of frequency down-converter devices using chirped RF modulated signal*, IEEE 36th VLSI Test Symposium (VTS) (2018)

²P. Sarson & al., *Measuring Group Delay of Frequency Downconverter Devices Using a Chirped RF Modulated Signal*, J. of Electronic Testing, **3**(34) 233–253 (2018)

³https://hpmwiki.mcguirescientificservices.com/_media/application_notes:an-1408-2.pdf

Complete reception chain calibration with respect to the GNSS simulator

- ▶ X310 input to 1-PPS input is measured using the oscilloscope (100 ps at 10 GS/s): **2930.8 ns**
- ▶ reference correlation peak recorded by the X310 with respect to the 1-PPS input: **7606.5 ns**.
- ▶ delay of the RF frontend: **17.3 ns**.
- ▶ GNSS simulator to measurement channels (E1 and E5a) of the X310s processed using `gnss-sdr` and the resulting pseudo-ranges are subtracted by the scenario configuring the simulator:
4663.1 ns

From this analysis, we compare the pseudo range delay to which the frontend delay and the reference output to reference input delays are added

$$4663.1 + 2930.8 + 17.3 = 7611.2$$

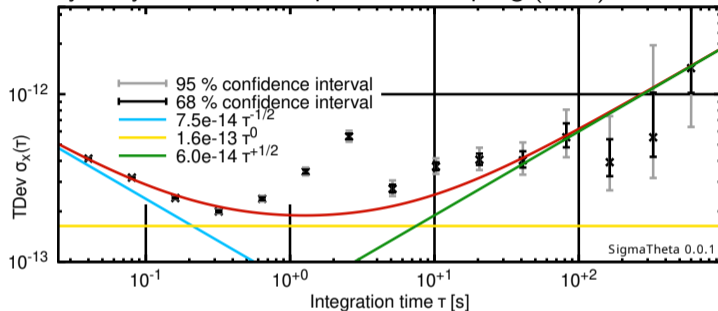
with the internal delay of reference signal referenced to the 1-PPS trigger

$$7611.2 - 7606.5 = 4.7 \text{ ns}$$

The leftover discrepancy of 4.7 ns is still under investigation but the strongest uncertainty on this analysis is the **validity of the mixer calibration**.

Conclusions

1. Ability to synchronize multiple direct sampling (ADC) SDR receivers with sub-ps resolution ⁴

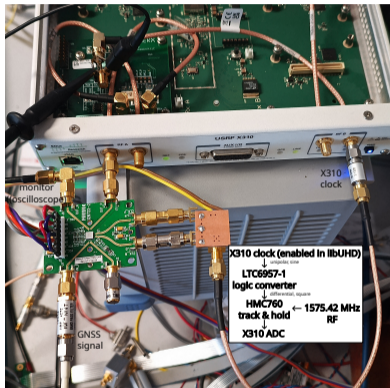
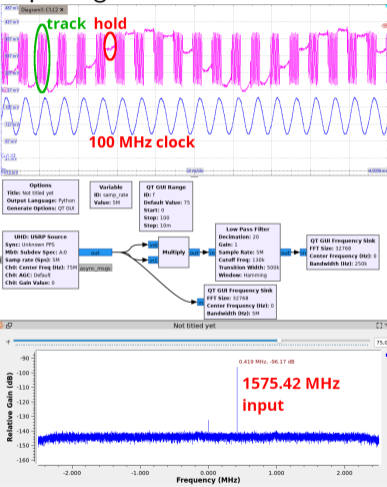


2. Full SNR resolution needed to achieve utmost performance \Rightarrow keep 14-bit samples
3. Select sampling rate only on GNSS considerations, reference PRN uses 2.5 Mchips/s BPSK = 5 MHz bandwidth \Rightarrow interpolation by peak fitting
4. Ability to calibrate with sub-100 ps resolution all linear components
5. Challenge of absolute calibration of mixer delay
6. Current processing power prevents real time processing of E^* and $L > 1 \Rightarrow$ record and post-process

⁴Complex frontends (AD9361, LMS7002) SDRs considerably degrade timing capability

Perspective

Replacing the mixer with a fast track & hold driven by ADC clock



Clock shaping from unbalanced to differential using a zero-crossing detector (LTC6957-1)

Update libuhd⁵ to enable clock output (false→true)

```
// disable TX dboard clock by  
// default  
this->get_iface()->set_clock_enabled  
(dboard_iface::UNIT_TX, false);
```

```
...  
this->get_iface()->set_clock_enabled  
(dboard_iface::UNIT_RX, false);
```

and provide as argument the clock rate

```
self.uhd_usrp_source_0 =  
uhd.usrp_source("".join((""  
'dboard_clock_rate=100E6')),  
uhd.stream_args(  
    cpu_format="fc32",  
    args='',  
    channels=list(range(0,1)),),)
```

⁵https://github.com/EttusResearch/uhd/blob/master/host/lib/usrp/dboard/db_basic_and_lf.cpp#L269