Analog to digital converters

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slides and references at `jmfriedt.free.fr`

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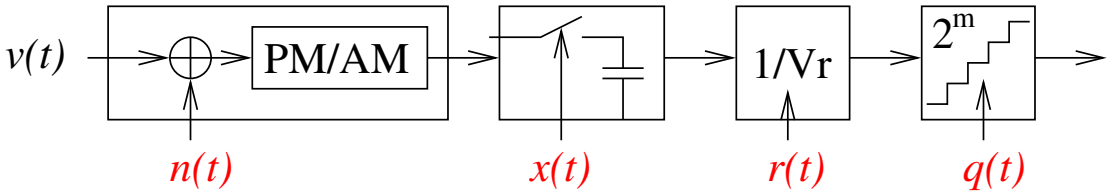
Basics

ADC: discrete time (aliasing) and discrete levels (quantization) [1]

$$V = V_{ref} \cdot \frac{bits}{2^m - 1} \Leftrightarrow bits = \frac{V}{V_{ref}} \cdot (2^m - 1)$$



- Characteristics: sampling rate and resolution
- 8 bits=48 dB dynamic range on input power ($20 \times \log_{10}(256)$)
- 10 bits=60 dB dynamic range on input power (Atmega32U4)
- 12 bits=72 dB dynamic range on input power
- 16 bits=96 dB dynamic range on input power
- V_{ref} noise directly impacts V measurement: $\frac{\Delta V_{ref}}{V_{ref}} = \frac{\Delta V}{V}$

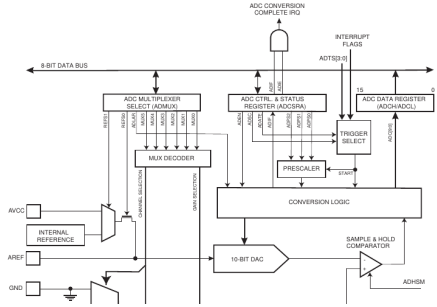
[1] C. Cardenas-Olaya, E. Rubiola, J.-M. Friedt, M. Ortolano, S. Micalizio, & C.E. Calosso, *Simple method for ADC characterization under the frame of digital PM and AM noise measurement*, Joint IFCS/EFTF (2015)

Technologies

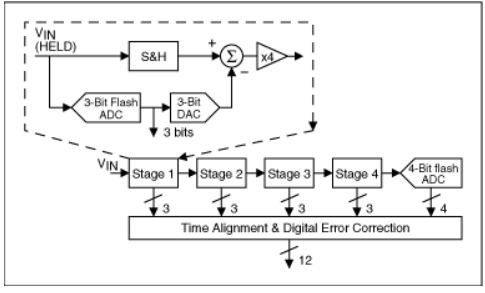
- successive approximation (SAR ADCs): as many clock cycles as bits on the output (low cost, low power)
- $\Sigma - \Delta$: 1-bit converter (comparator) followed by low-pass filtering (audiofrequency, very high resolution thanks to oversampling)
- flash: voltage ladder with comparator, for very fast (>100 MS/s) ADC
- pipelined ADC: mix between successive approximation and flash ADC (fast but introduces some latency, higher resolution than single-flash)

+dithering

Figure 24-1. Analog to Digital Converter Block Schematic



Atmega32U4 datasheet

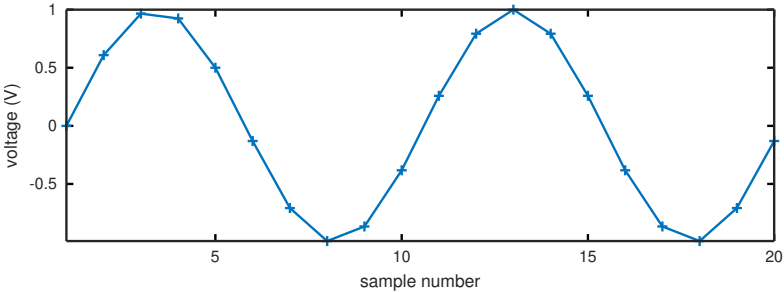


Maxim APP1023 application note

Identifying the sampling rate from continuous acquisition

Signal generated at 20 kHz

Unknown sampling rate, continuous output stream



What is the sampling rate ? resolution ?

Identifying the sampling rate from continuous acquisition

Signal generated at 20 kHz

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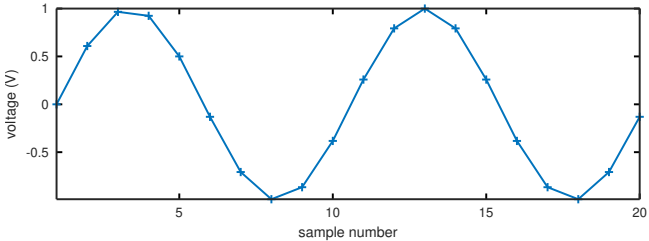
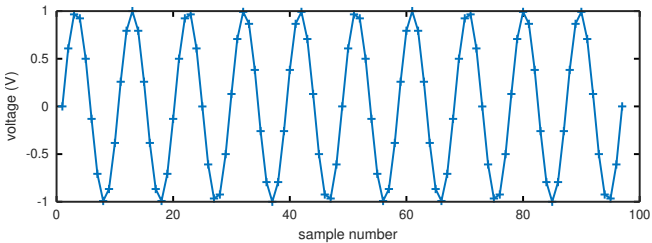
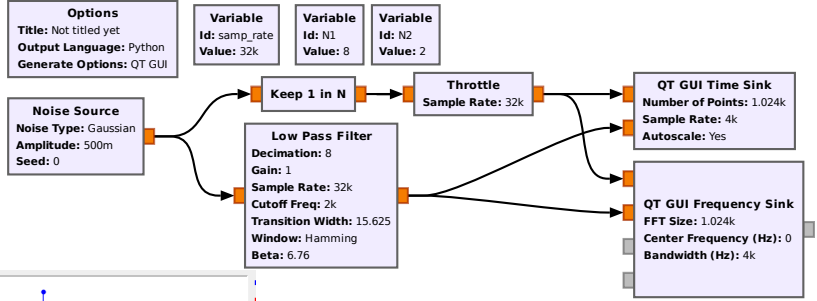
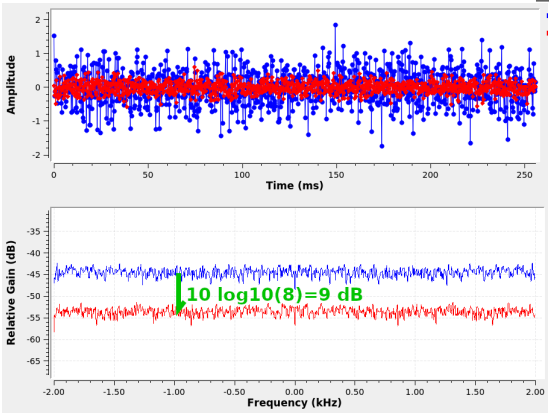




What is the sampling rate ? resolution ?

Noise aliasing



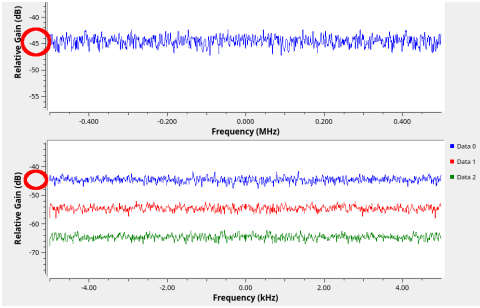


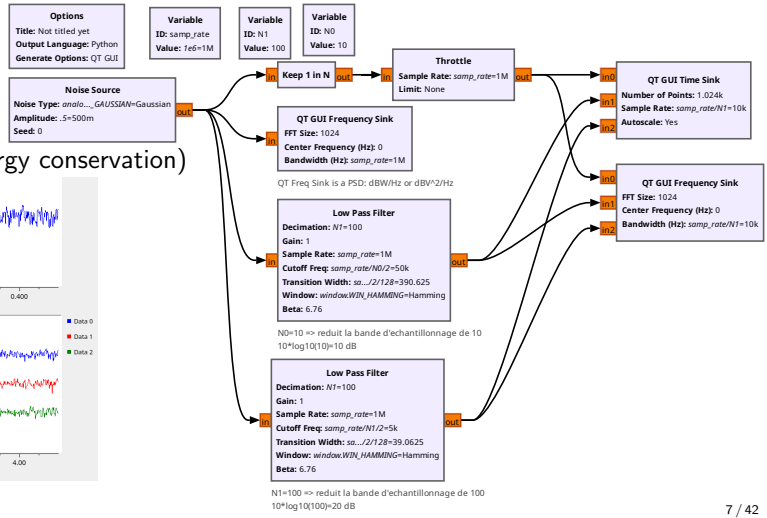
- low-pass filter before sampling to remove unwanted alias
- low-pass filter before sampling to reject out-of-band noise
- if only baseband sampling of broadband noise: energy conservation accumulates noise in baseband by aliasing $\Rightarrow$ raises noise floor

Noise aliasing

Notice the GNU Radio QT Frequency Sink block is a **Power Spectral Density** (PSD) display in dBW/Hz or dBV^2/Hz:

- Same asymptotic level before or after decimation by 10 or 100
- Power spectral density rises when decimating with respect to displaying the full bandwidth (energy conservation)





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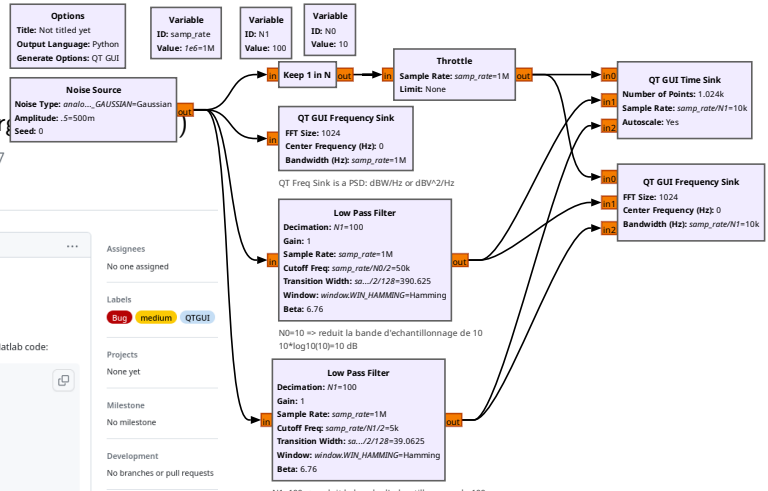


scaling in Qt Frequency Sink wrong #4827

Open ali69550 opened this issue on Jun 30, 2021 · 11 comments

ali69550 commented on Jun 30, 2021 • edited by dkozel

Hi,
In the code of "freq_sink_c_impl.cc" there is a problem:
instead of averaging `abs(fft())^2` and then taking the logarithm,
it first calculates the logarithm of `abs(fft())^2` and then averages!
as we all know `log(a + b) != log(a) + log(b)` .
This causes a 2.5 dB lower result that can be easily shown by the following simple Matlab code:

```
M = 4; % M-PSK
L = 10000; % no. of averages
Nfft = 2000; % fft size
N = Nfft * L;
sbi_v = randi(M, N, 1) - 1; % integer symbols
sbc_v = pskmod(sbi_v, M, pi/4, 'gray'); % complex symbols
sbc_m = reshape(sbc_v, Nfft, N/Nfft);
SBC_m = abs( fft(sbc_m, Nfft) ).^2;
SBC_log_m = 10*log10(SBC_m);
plot( [mean( SBC_log_m, 2) 10*log10( mean( SBC_m, 2) )] )
grid on
```

Assignees
No one assigned

Labels
Bug medium QTGUI

Projects
None yet

Milestone
No milestone

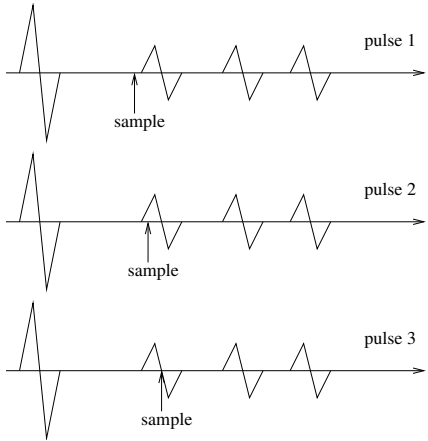
Development
No branches or pull requests

Notifications

Sample & hold

- Sample & hold (Track & hold): input stage for keeping the sampled voltage constant
- Defines the bandwidth over which noise is integrated
- Possibly much higher than the sampling (conversion) rate

Example of external Track&Hold control:
Linear Technology LTC1407 (see also LTC2145 datasheet: 750 MHz T&H for 125 MS/s ADC)
Application to **stroboscopic** measurements[2]:
100 MHz carrier, echo delays at 1.2 and 1.5 μs,
4 GS/s equivalent sampling rate **assuming** stationary environment



[2]F. Minary, D. Rabus, G. Martin, J.-M. Friedt, *Note: a dual-chip stroboscopic pulsed RADAR for probing passive sensors*, Rev. Sci. Instrum. **87** p.096104 (2016)

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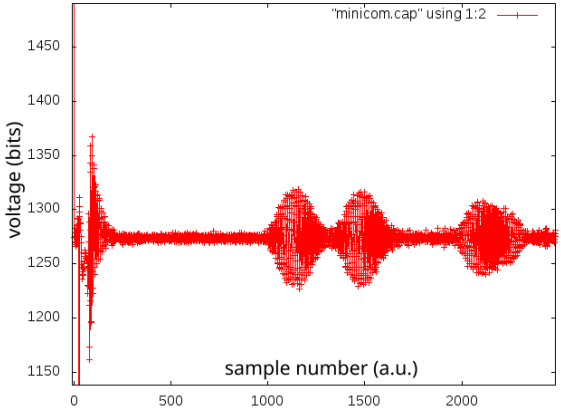

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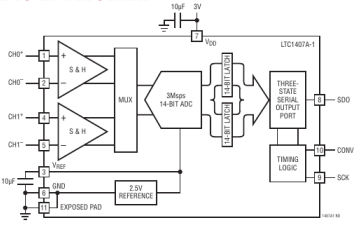
BLOCK DIAGRAM



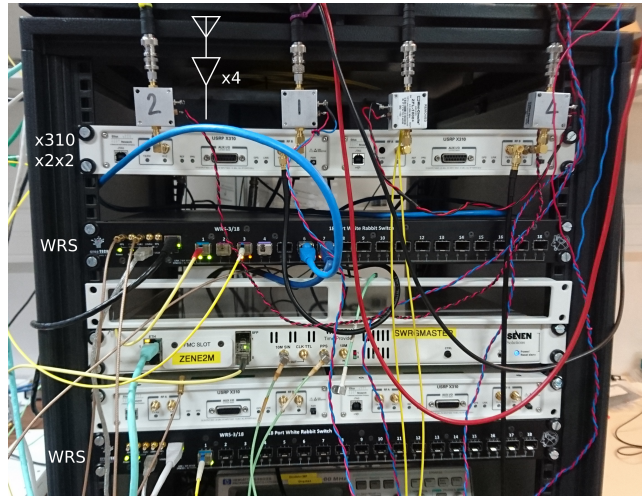
ANALOG INPUT The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With internal reference, V_{DD} = 3V.

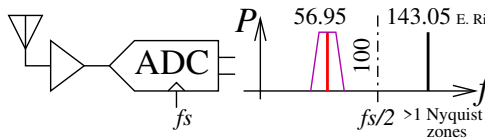
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Differential Input Range (Notes 3, 8, 9)	2.7V ≤ V_{DD} ≤ 3.3V			–1.25 to 1.25		V
V_{CM}	Analog Common Mode + Differential Input Range (Note 10)				0 to V_{DD}		V
I_{IN}	Analog Input Leakage Current		●			1	µA
C_{IN}	Analog Input Capacitance	(Note 18)			13		pF
t_{ACQ}	Sample-and-Hold Acquisition Time	(Note 6)	●			39	ns
t_{AP}	Sample-and-Hold Aperture Delay Time				1		ns
t_{JITTER}	Sample-and-Hold Aperture Delay Time Jitter				0.3		ps
t_{SK}	Sample-and-Hold Aperture Skew from CH0 to CH1				200		ps

[2] F. Minary, D. Rabus, G. Martin, J.-M. Friedt, *Note: a dual-chip stroboscopic pulsed RADAR for probing passive sensors*, Rev. Sci. Instrum. **87** p.096104 (2016)

Aliasing for distributed RADAR

- Ettus Research X310: 200 MS/s ADC
- BasicRX daughter board: 1–250 MHz passive balun feeding the ADC
- Sub-sampling the 143.05 MHz at 200 MS/s: uses second Nyquist zone and aliased signal appears at $|100 - 43.05| = 56.95$ MHz
- Multiple USRP sources: all X310 must be controlled by the same computer running GNU Radio (connected to the same subnetwork)
- From `samp_rate`=1.536 MS/s to 768 Hz: cascaded FIR filters decimating by 20, 5 and 20 respectively ending with an 800 Hz cutoff frequency
- *assumes* no signal in aliases of 143.05 MHz $\pm$ 800 Hz





E. Richter, Usage of higher order Nyquist Zones with direct sampling Devices https://www.youtube.com/watch?v=PI_ROLXqO_Q

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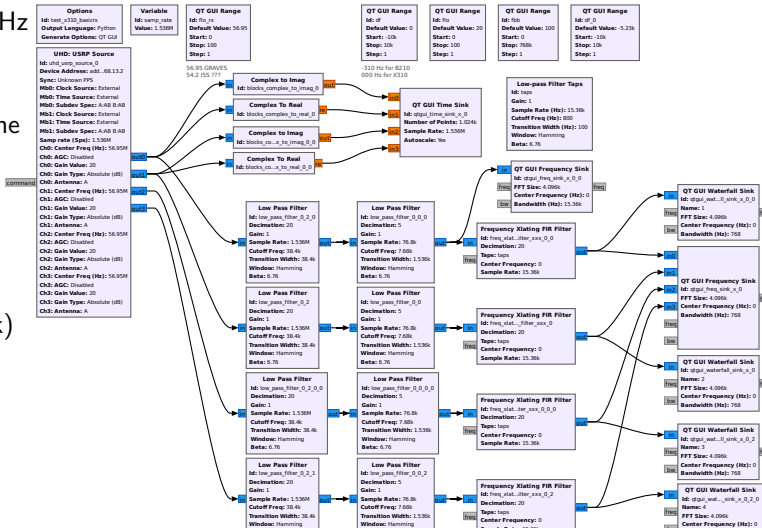
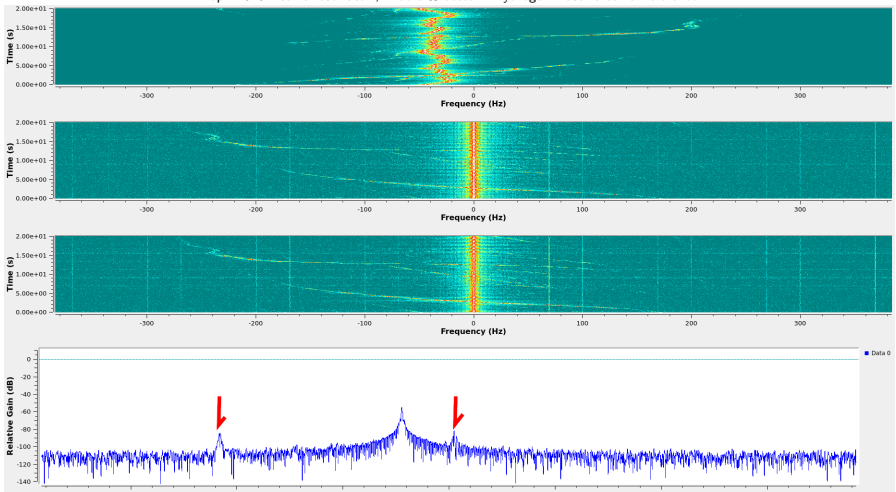


Impact of local oscillator stability

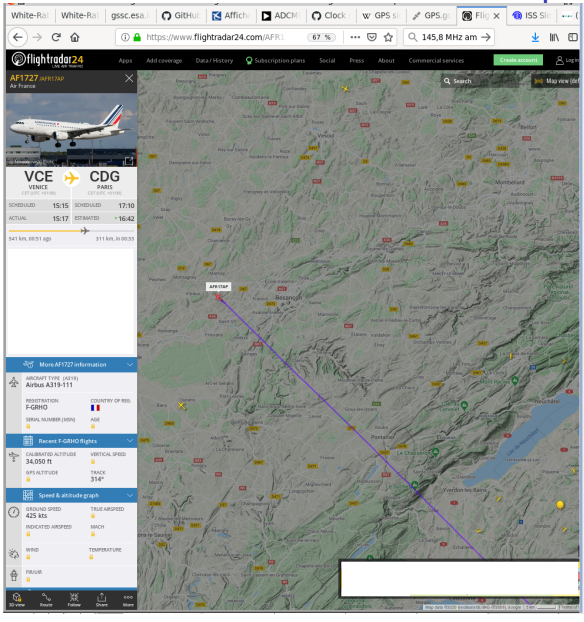
Need for stable local oscillator: 300 Hz @ 143 MHz = 2 ppm long term stability

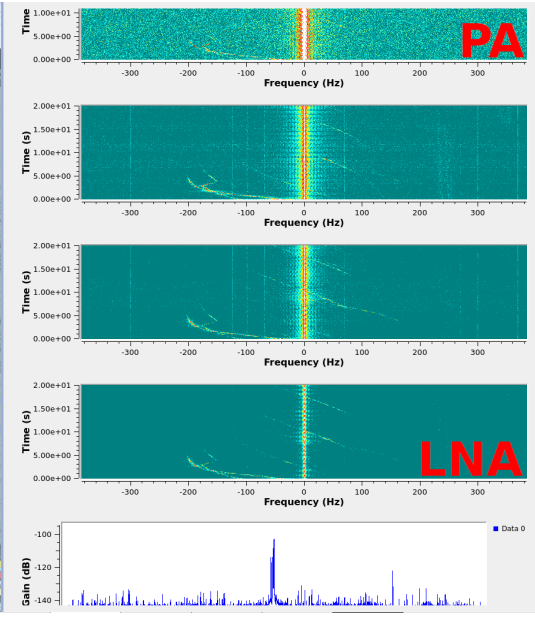
Top: X310 internal oscillator ; middle & bottom: hydrogen maser external reference



- each moving target is identified with a different Doppler shift after FFT of the recorded signal
- low streaming datarate: 600 S/s sufficient, 1 kS/s safe

Results: 2 km ENSMM-UFR ST optical fiber between WRS





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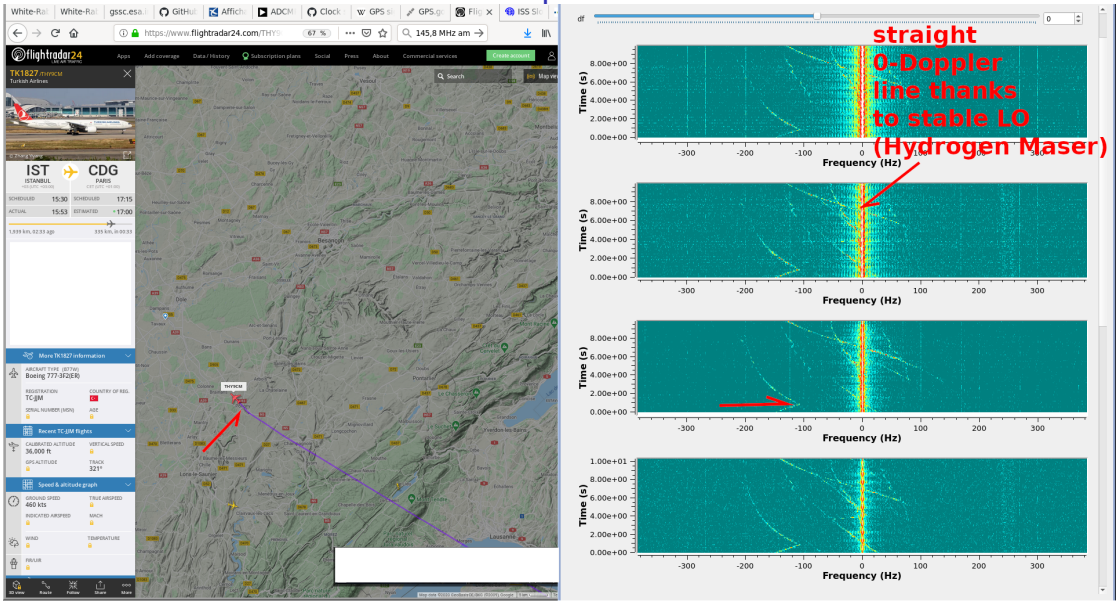


Impedance and equivalent circuit

From the Atmega32U4 datasheet (section 24.7.1):

Analog Input Circuitry

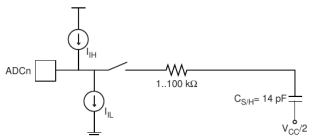
The analog input circuitry for single ended channels is illustrated in Figure 24-9. An analog source applied to ADCn is subjected to the pin capacitance and input leakage of that pin, regardless of whether that channel is selected as input for the ADC. When the channel is selected, the source must drive the S/H capacitor through the series resistance (combined resistance in the input path).

The ADC is optimized for analog signals with an output impedance of approximately 10kΩ or less. If such a source is used, the sampling time will be negligible. If a source with higher impedance is used, the sampling time will depend on how long time the source needs to charge the S/H capacitor, with can vary widely. The user is recommended to only use low impedance sources with slowly varying signals, since this minimizes the required charge transfer to the S/H capacitor.

If differential gain channels are used, the input circuitry looks somewhat different, although source impedances of a few hundred kΩ or less is recommended.

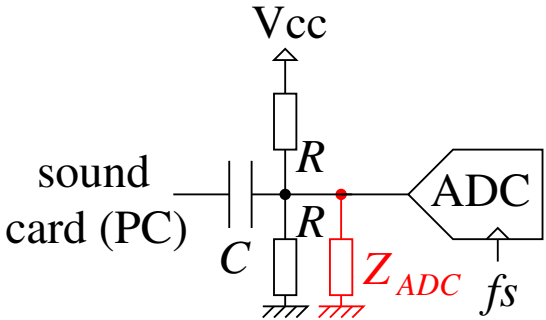
Signal components higher than the Nyquist frequency ($f_{ADC}/2$) should not be present for either kind of channels, to avoid distortion from unpredictable signal convolution. The user is advised to remove high frequency components with a low-pass filter before applying the signals as inputs to the ADC.

Figure 24-9. Analog Input Circuitry



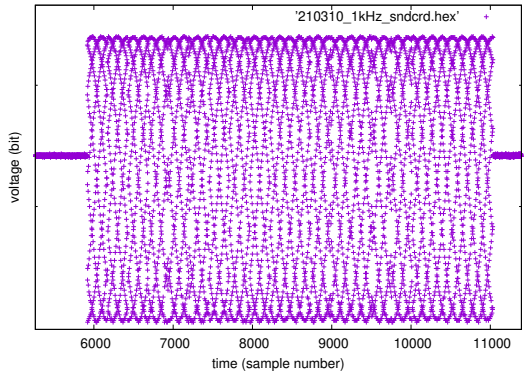
- Typical ADC equivalent impedance: $\simeq 10$ kΩ
- Make sure sensor impedance is $\ll 10$ kΩ, otherwise voltage divider between sensor impedance and ADC impedance
- operational amplifier as follower acts as impedance buffer (high input impedance, low output impedance)
- select single supply or rail to rail operational amplifier for positive power supply only

Impedance and equivalent circuit



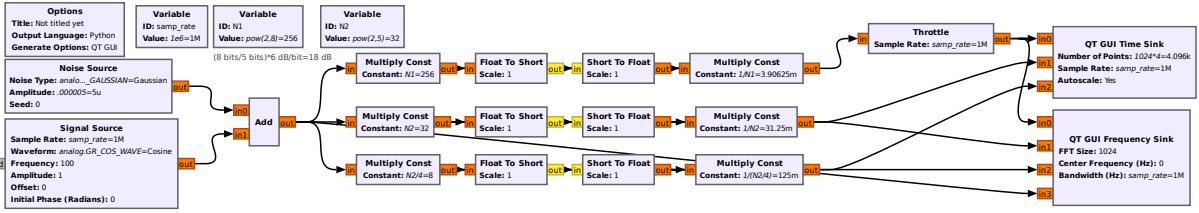
Bias T layout:

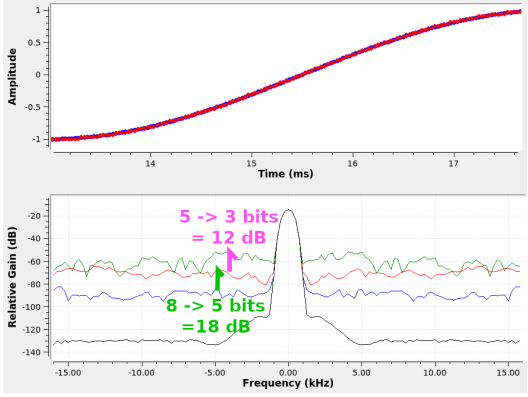
- sound card output centered on 0 V, but ADC can only sample from 0 to V_{ref}
- C impedance $|Z_C| = 1/(C\omega)$ must be much lower at $\omega = 2\pi f$ than resistor bridge impedance
- R much lower than Z_{ADC} (resistor bridge divider assumption)



- at 1 kHz, 100 nF: $Z_{100nF} = 1600\ \Omega \ll Z_{ADC}$
- $R \ll Z_{ADC}$ but $R \geq Z_C$: $R \simeq 2200..5600\ \Omega$

Quantization noise floor





- add noise ($5 \cdot 10^{-6}$) over a full-scale (1) range sine wave ("noise dithering" over sine wave – noise only will be below LSB)
- $20 \cdot \log_{10}(2) = 6.02$ dB/bit resolution impacts on noise floor

Averaging for improved resolution

- Noise scales as $1/\sqrt{M}$ when averaging over M samples $\Rightarrow$ 4-times sampling rate loss for 1-additional bit
- $10\log_{10}(4) = 6.02$ dB/bit

Which input interface is better for sampling a 77500 Hz signal ? a 16-bit sound card sampling at 192 kS/s or a 8-bit DVB-T sampling at 2 MS/s ?

Averaging for improved resolution

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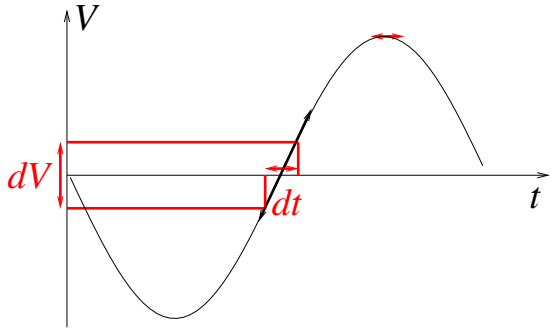
Which input interface is better for sampling a 77500 Hz signal ? a 16-bit sound card sampling at 192 kS/s or a 8-bit DVB-T sampling at 2 MS/s ?

$f_{ss} = 4^p \times f_s \Leftrightarrow 10\log_{10}(f_{ss}/f_s) = 10\log_{10} 4 \times p \simeq 6.02 \times p$
i.e. $10\log_{10}(\underbrace{10}_{2\cdot 10^6/192000})/6.02 \simeq 1.5$ bits: high sampling rate only gains 1.5 bit or 9.5 bit equivalent, poorer than sound card (16 bit) result

Impact of clock jitter

- jitter impact dependent on fastest slope of signal
- minimum impact at signal maximum (amplitude fluctuations)



$v(t) = A \cdot \cos(\omega t) \Rightarrow \max(dv/dt) = A\omega$

Jitter $\tau \Rightarrow dv = A\omega\tau \Rightarrow \sigma_v = A\omega\sigma_\tau$ & $\tau = \varphi/\omega \Rightarrow \sigma_v = A\sigma_\varphi$

Impact of clock jitter

AD9228

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR\ Degradation = 20 \times \log 10(1/2 \times \pi \times f_A \times t_J)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter. IF undersampling applications are particularly sensitive to jitter (see Figure 57).

ERROR:

$$SNR_{degradation} = -20\log_{10}(2\pi f_{in}\sigma_\tau)$$

ANALOG DEVICES

Quad, 12-Bit, 40/65 MSPS
Serial LVDS 1.8 V A/D Converter

Data Sheet AD9228

FEATURES

- 4 ADCs integrated into 1 package
- 119 mW ADC power per channel at 65 MSPS
- SNR = 70 dB (to Nyquist)
- ENOB = 11.3 bits
- SFDR = 82 dBc (to Nyquist)
- Excellent linearity
  - DNL = ±0.3 LSB (typical)
  - INL = ±0.4 LSB (typical)
- Serial LVDS (ANSI-644, default)
  - Low power, reduced signal option (similar to IEEE 1596.3)
- Data and frame clock outputs
- 315 MHz full-power analog bandwidth
- 2 V p-p input voltage range
- 1.8 V supply operation
- Serial port control
  - Full-chip and individual-channel power-down modes
  - Flexible bit orientation
  - Built-in and custom digital test pattern generation
  - Programmable clock and data alignment
  - Programmable output resolution

FUNCTIONAL BLOCK DIAGRAM

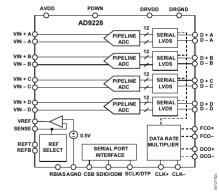


Figure 1.

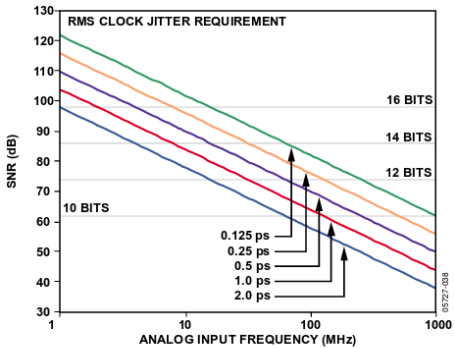
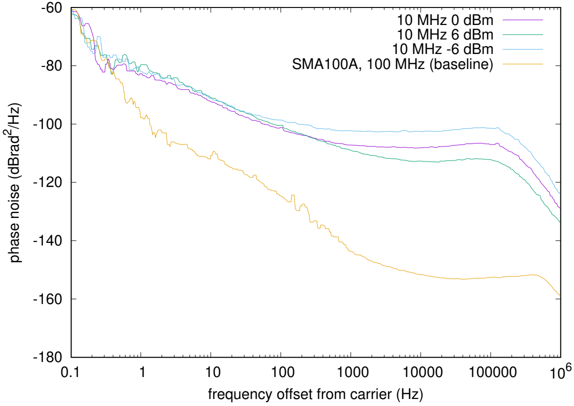


Figure 57. Ideal SNR vs. Input Frequency and Jitter

Application example: sound card

1. **Assume a local oscillator with $S_\varphi = -110$ dBrad^2/Hz phase white phase noise**
2. **Assume a 16 (or 24) bit ADC clocked at 192 kHz operating in ± 1 V range**
3. **Impact of clock jitter on a 10 kHz input signal at full scale range ?**



ar electronique — CRYSTAL OSCILLATORS - VOLTAGE CONTROLLED CRYSTAL OSCILLATORS — **XO - VCXO**

FREQUENCY RANGE (MHz): 5, 30, 90, 150, 270, 2000 — FREQUENCY STABILITY vs TEMP. (+/-): 5.10-6, 10.10-6, 20.10-6, 30.10-6, 50.0-6 — Fcy vs CONTROL VOLTAGE (+/-): 10.10-6, 20.10-6, 30.10-6, 50.10-6, 100.10-6, 300.10-6, 500.10-6, 5000.10-6

FAMILY	Temp. range	EXAMPLE	100 Hz	1 KHz	10 KHz	100 KHz	5V	12V / 15V	SINE	LOGIC	2121 AM 11	2736 BM 10	Milled	
OBTAR	[+10, +40]°C	100 MHz												Quartz resonator
	[0, +50]°C	Std	-115	-142	-155	-155	O	S	S	O	S	O	S	very low phase noise
	[-10, +60]°C	Option	-120	-150	-160	-165								
OBTAR-H	[-20, +70]°C													Quartz resonator, 5th to 9th O.T.
	[-40, +95]°C	1 GHz	-100	-125	-140	-145		S	S				S	internal multiplier
	[-55,+100]°C													low phase noise
VCLI		20 MHz +/- 5.10-3	-80	-110	-135	-155	O	S	S	O	S	S	S	Lithium tantalate resonator wide frequency shift
VCSI		20 MHz +/- 200.10-6	-120	-150	-155	-155	O	S	S	O	S	O	S	Quartz resonator low to medium frequency shift
VCSI-H		1 GHz +/- 50.10-6	-95	-120	-140	-145		S	S				S	Quartz resonator, 5th to 9th O.T. internal multiplier low phase noise

Notes :
- A.R.Electronique crystal resonators manufacturing ;
- military / avionic versions available (low g sensitivity) ;
- detailed information : please ask for particular data sheet.

Legend :
S : standart
O : option

http://www.ec-m.it/docs/XO-VCXO.pdf

Application example: sound card

1. **Assume a local oscillator with $S_\varphi = -110$ dBrad^2/Hz phase white phase noise**
2. **Assume a 16 (or 24) bit ADC clocked at 192 kHz operating in ± 1 V range**
3. **Impact of clock jitter on a 10 kHz input signal at full scale range ?**

- $S_\varphi = \frac{\sigma_\varphi^2}{B}$ with B integration bandwidth and σ_φ phase standard deviation:
  $\sigma_\varphi = \sqrt{10^{S_\varphi/10} \times B} = 1.4 \cdot 10^{-3}$ rad if $B = f_{ADC}$

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- $2\pi \times 10000 \times 1.2 \cdot 10^{-9} = 75\ \mu$V: 16 bit ADC lost 1 bit and prevents full resolution of 24 bit ADC (only 15 bits valid)
- to keep all significant bits of the 16-bit ADC, a noise floor of -118 dBrad^2/Hz at least would be needed
- to keep all significant bits of the 24-bit ADC, a noise floor of -166 dBrad^2/Hz at least would be needed

Application example: RF ADC

1. **Assume a local oscillator with $S_\varphi = -110$ dBrad^2/Hz phase white phase noise**
2. **Assume a 12 (or 16) bit ADC clocked at 125 MHz operating in ± 1 V range**
3. **Impact of clock jitter on a 5 MHz input signal at full scale range ?**

Application example: RF ADC

1. **Assume a local oscillator with $S_\varphi = -110$ dBrad^2/Hz phase white phase noise**
2. **Assume a 12 (or 16) bit ADC clocked at 125 MHz operating in ± 1 V range**
3. **Impact of clock jitter on a 5 MHz input signal at full scale range ?**

- $S_\varphi = \frac{\sigma_\varphi^2}{B}$ with B integration bandwidth and σ_φ phase standard deviation:
  $\sigma_\varphi = \sqrt{10^{S_\varphi/10} \times B} = 35$ mrad if $B = f_{ADC}$

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- $2\pi \times 5 \cdot 10^6 \times 45 \cdot 10^{-12} = 1.4$ mV: only 10.5 significant bits
- a noise floor of -143 dBrad^2/Hz would be needed to keep all 16-bits (0.8 mrad $\rightarrow$ 1 ps $\rightarrow$ 31 μV)

Bibliography

- Clock and voltage reference statistical noise impacts on ADC output stability.
- High bandwidth ADC needed for high frequency signals
- If low frequency signals, resolution is improved by averaging ...
- but low frequency ADCs usually provide more bits.
- Adding noise before averaging can improve resolution !

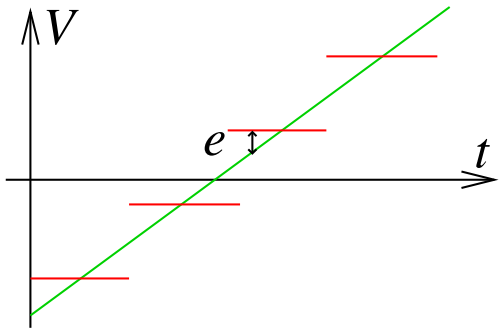
[1] M. Bellanger, *Traitement numérique du signal : Théorie et pratique, 8e Ed.*, Sciences Sup, Dunod (2012)
[2] B. Widrow & I. Kollár, *Quantization Noise: Roundoff Error in Digital Computation, Signal Processing, Control, and Communications*, Cambridge University Press (2008)
[3] B. Morley, *ESE488 Signals and Systems Laboratory* (2016), `classes.engineering.wustl.edu/ese488/Lectures/Lecture5a_QNoise.pdf`
[4] PhD Carolina Cárdenas Olaya, *Digital Instrumentation for the Measurement of High Spectral Purity Signals* (2017), at `http://porto.polito.it/2687860/1/Polito_PhD_Thesis.pdf`
[5] P.-Y. Bourgeois, T. Imaike, G. Goavec-Merou & E. Rubiola, *Noise in High-Speed Digital-to-Analog Converters*, IFCS 2015

Quantization noise

- samples are uniformly distributed from $-q/2$ to $+q/2$ with q the quantization step
- quantization error e distribution

$$\sigma_v^2 = E(e^2) = \frac{1}{q}\int_{-q/2}^{+q/2} e^2 \cdot de = \frac{1}{q}\left[\frac{e^3}{3}\right]_{-q/2}^{+q/2} = \frac{1}{q}\left(\frac{q^3}{3\times 8} - \frac{-q^3}{3\times 8}\right)$$

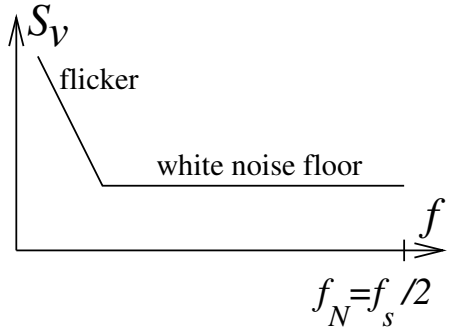
$$= \frac{1}{q}\left(\frac{2q^3}{24}\right) = \frac{q^2}{12}$$



ENOB

$$\frac{S_v \text{ dBV}^2/\text{Hz} \times f_s}{6.02 \text{ bit/dB}} = \text{ENOB} = \log_2\left(1 + \frac{V_{FSR}}{\sqrt{12 \cdot f_N \cdot S_{floor}}}\right)$$

Measurement: 50Ω load or sine wave on both channels and subtract measurements (remove impact of common track & hold jitter)



ENOB: Effective Number Of Bits

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$v_q = \frac{v_{fsr}}{2^M - 1}$: here the target is M =ENOB.

$$\sigma^2 = \frac{v_q^2}{12}$$

then the total noise density over the bandwidth is $\mathcal{N}_t = \frac{\sigma^2}{fs}$

Now we express

$$\sqrt{\mathcal{N}_t} = \frac{\sigma}{\sqrt{f_s}} = \frac{v_q}{\sqrt{12 f_s}} = \frac{v_{fsr}}{\sqrt{12 \cdot fs}(2^M - 1)} \text{ so } 2^M = 1 + \frac{v_{fsr}}{\sqrt{12 \cdot fs \cdot \mathcal{N}_t}}$$

$$\Rightarrow ENOB = M = \log_2\left(1 + \frac{v_{fsr}}{\sqrt{12 \cdot f_s \cdot \mathcal{N}_t}}\right)$$

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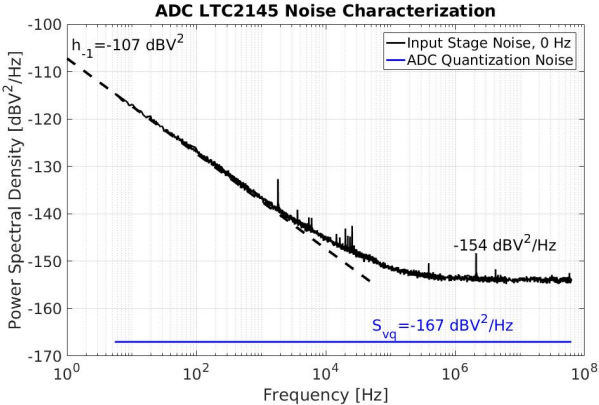

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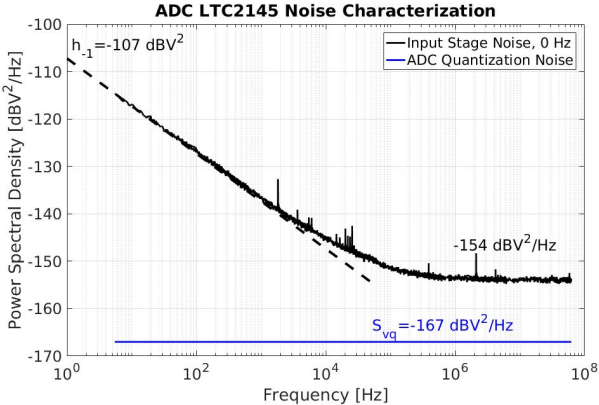
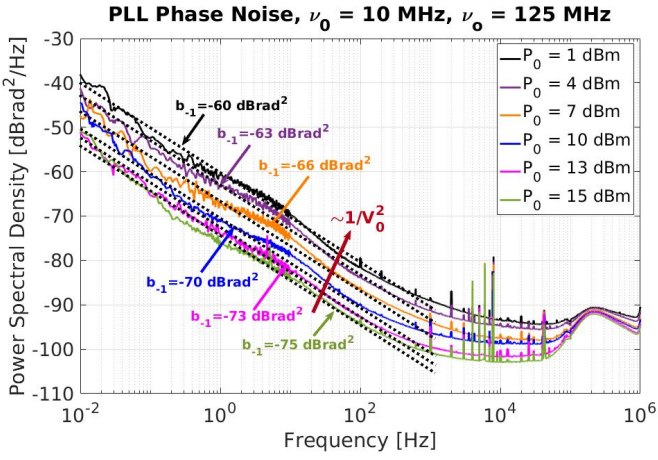


2 V ref, 14 bit ADC: $14 \times 6.02 + 10 \cdot \log_{10}(125 \cdot 10^6) + 10 \cdot \log_{10}(2) = 168$ dBV^2/Hz ideally
but $(-154 + 10 \cdot \log_{10}(125 \cdot 10^6) + 1.76)/6.02 = 11.8$ bits practically

Oscillator phase noise



(a) Input carrier frequency $\nu_0 = 10$ MHz.

PhD Carolina Cárdenas Olaya, *Digital Instrumentation for the Measurement of High Spectral Purity Signals* (2017), at `http://porto.polito.it/2687860/1/Polito_PhD_Thesis.pdf`

$$\sigma_\varphi^2 = S_\varphi \cdot BW = BW \cdot 10^{S_\varphi(dB)/10}$$

Low-pass filtering the ADC measurements

- IIR: $\sum a_k y_{n-k} = \sum b_k x_{n-k}$
- FIR: $y_n = \sum b_k x_{n-k}$
- Delay dependent on N number of coefficients, bits per sample ?